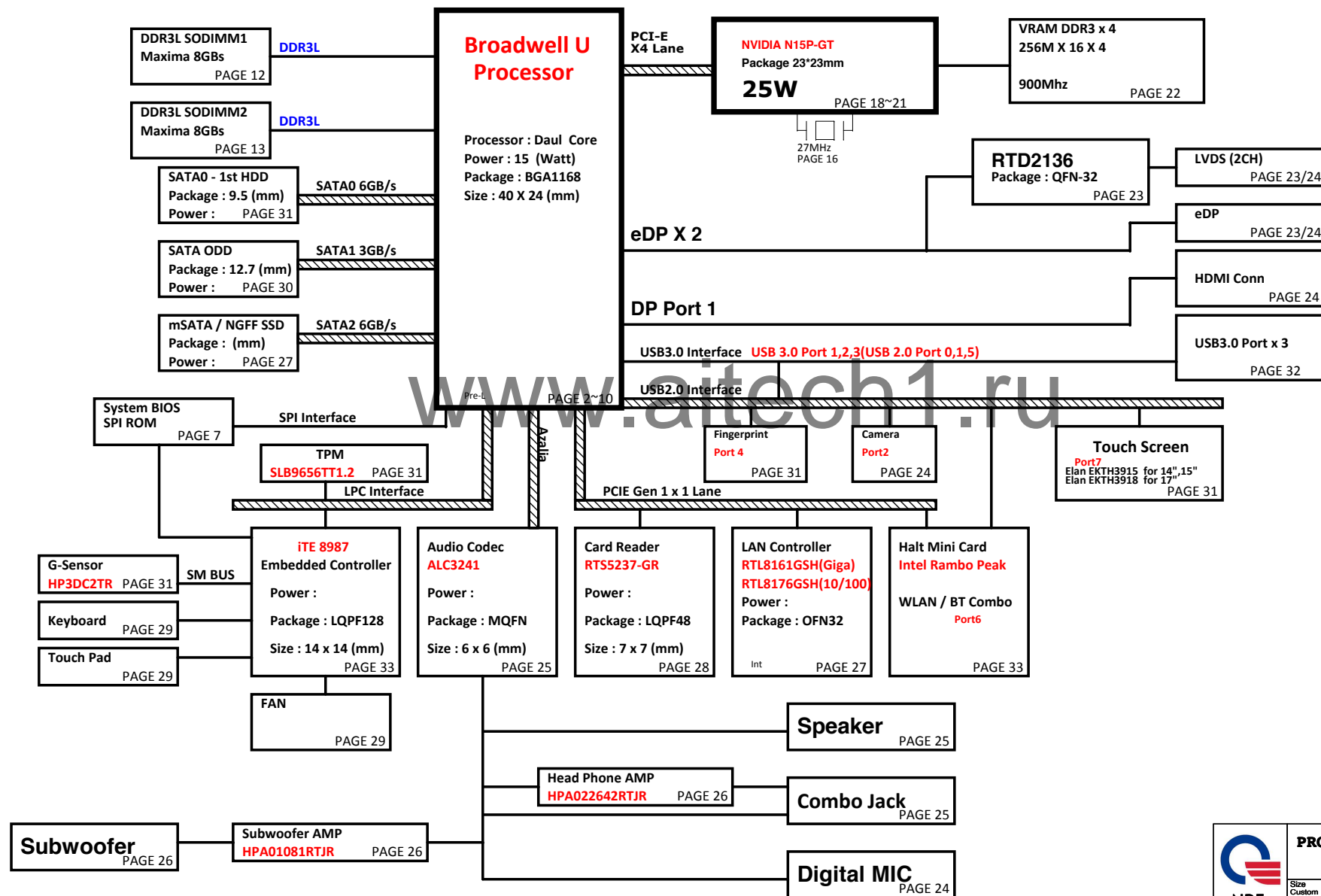
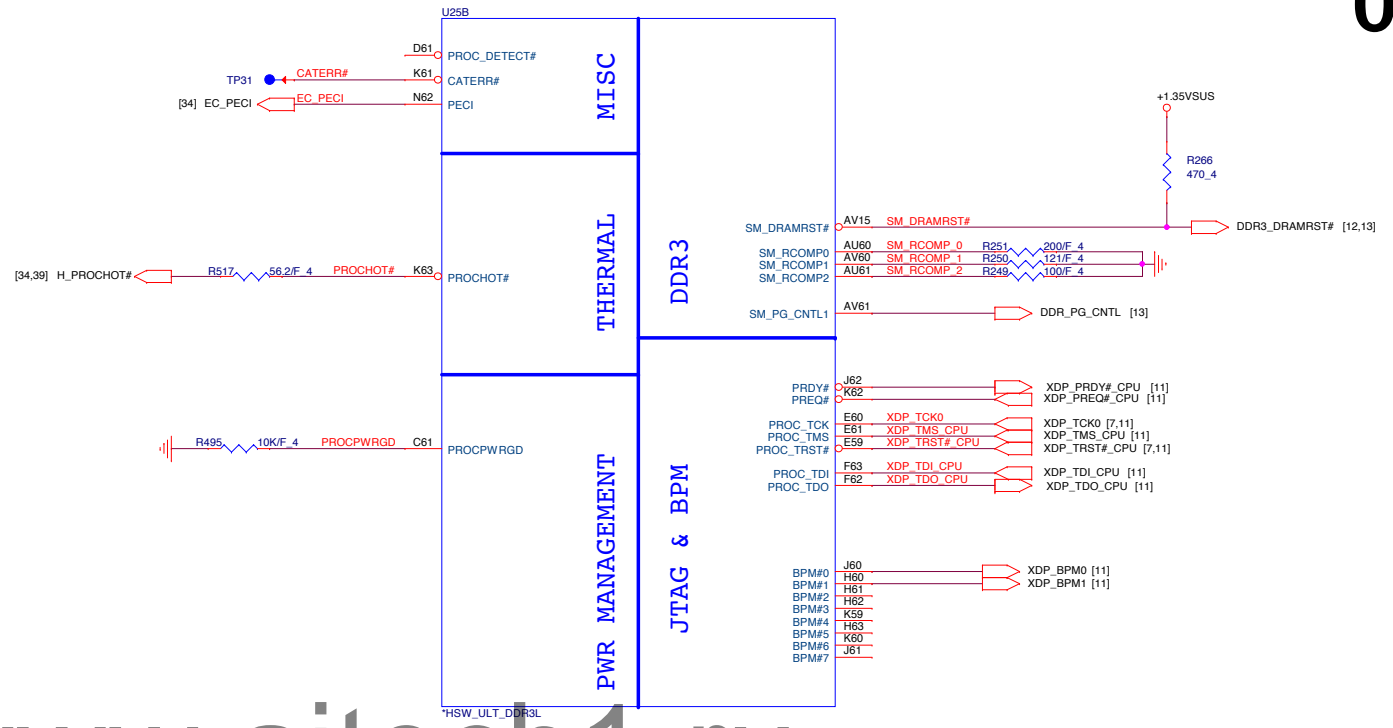
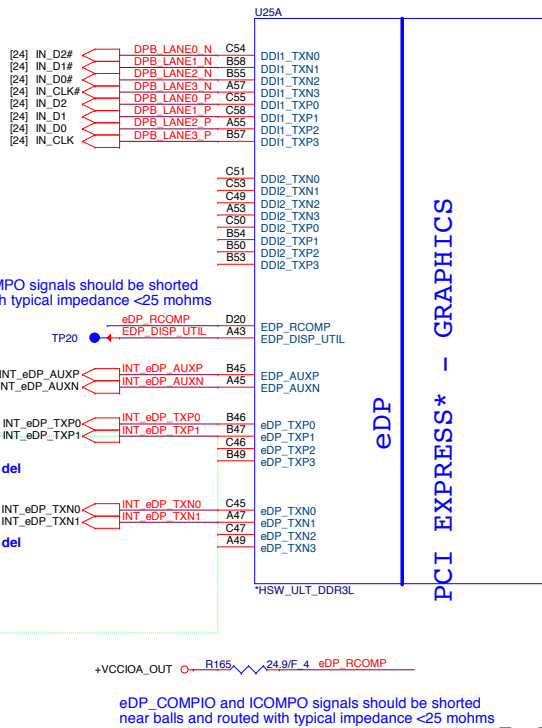


# DIS (14" / 15" / 17") Lay-Vine Intel Crescent Bay ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT





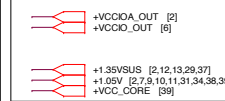
www.aitech1.ru

**DDR SYSTEM MEMORY A**

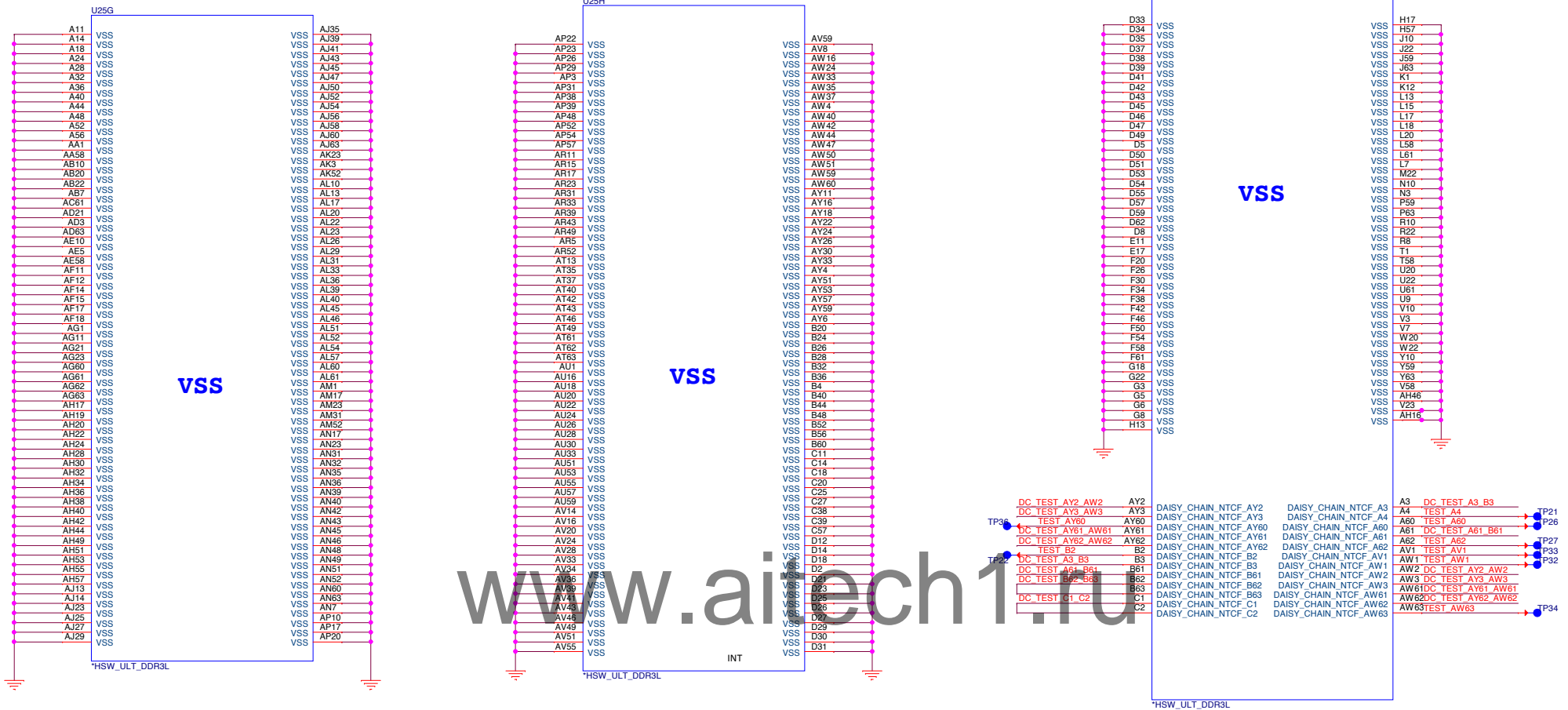
**DDR SYSTEM MEMORY B**

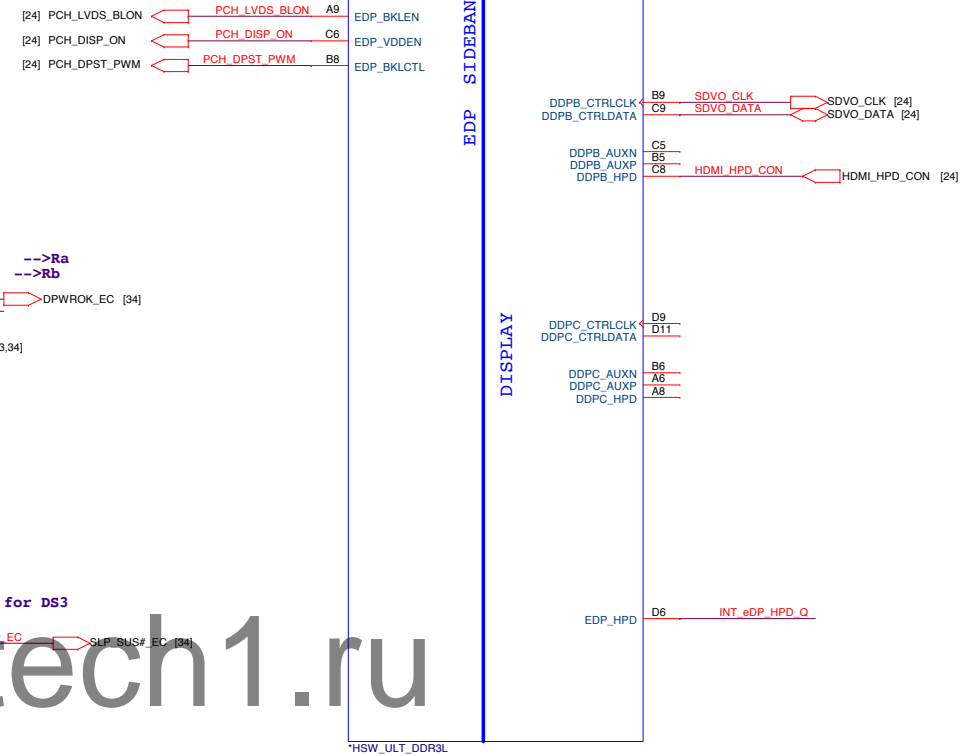
**PROJECT : Y11C**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	ULT 2/9 (DDR3 I/F)	1A
Date: Tuesday, September 02, 2014		Sheet 3 of 44



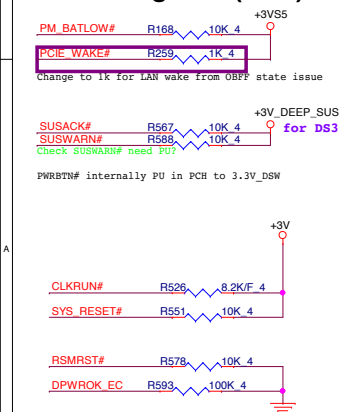




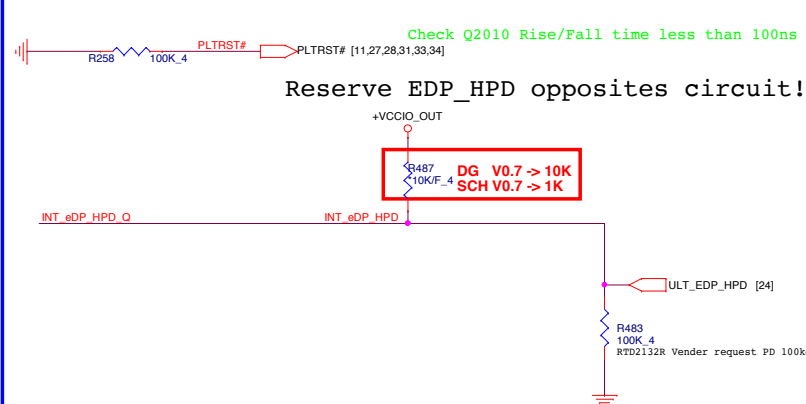


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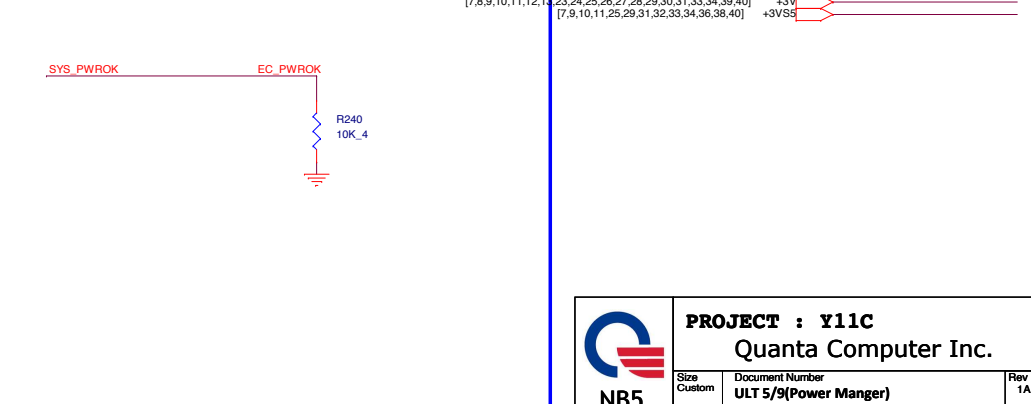
## PCH Pull-high/low(CLG)






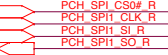
## PLTRST#(CLG)



## System PWR\_OK(CLG)

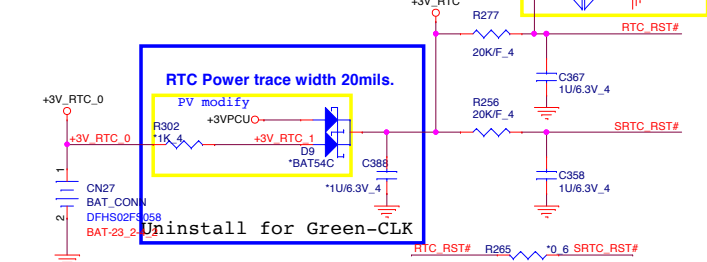


[illegible]

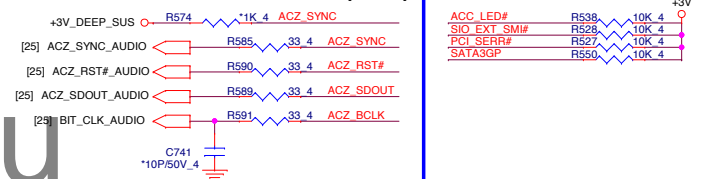
Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTCO 						
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden	[34] GPIO33_EC 						
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"> <thead> <tr> <th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>LPC</td></tr> <tr> <td>0</td><td>SPI(Default)</td></tr> </tbody> </table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTCO 						
				<div> <div> [34] PCH_SPI_CS0#_R  [34] PCH_SPI1_CLK_R  [34] PCH_SPI1_SI_R  [34] PCH_SPI1_SO_R </div>  </div>						

no stuff If use green Clock

### RTC Circuitry(RTC)



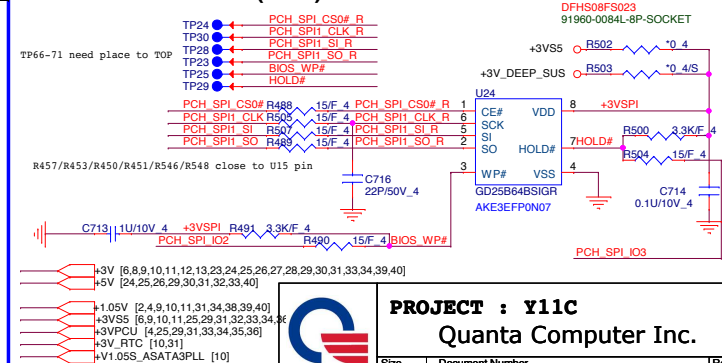
## GPIO Pull UP



Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

U10&U15 footprint 要重疊

## PCH SPI ROM(CLG)

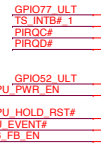
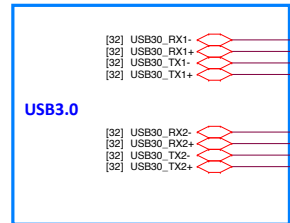
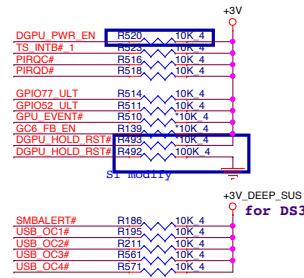


**PROJECT : Y11C**  
Quanta Computer Inc.

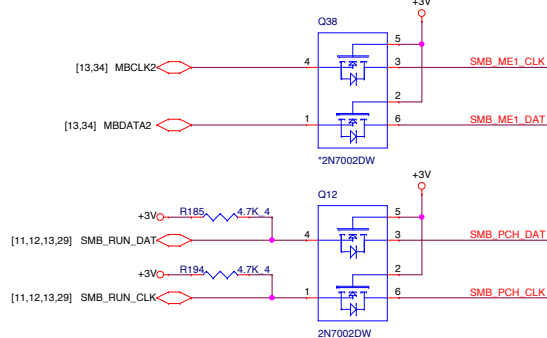
Size Custom	Document Number <b>ULT 6/9(SATA/HDA)</b>	Rev 1A
Date: Tuesday, September 02, 2014	Sheet 7 of	44

# Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

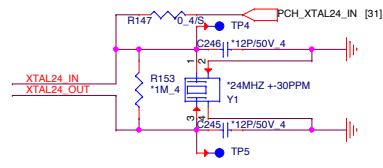
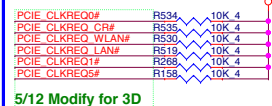
## PCI/USBOC# Pull-up(CLG)



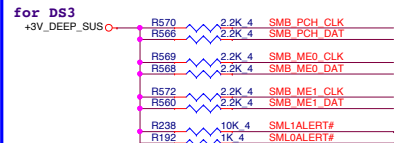
## SMBus/Pull-up(CLG)



## CLK\_REQ/Strap Pin(CLG)



## SMBus/Pull-up(CLG)

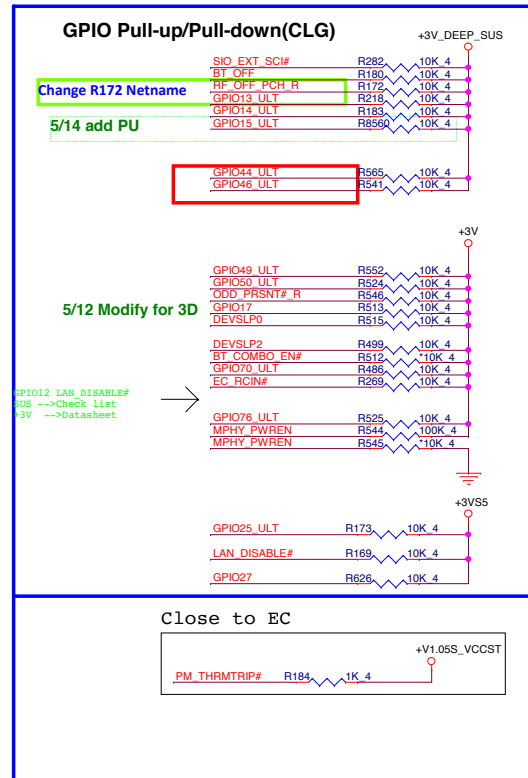
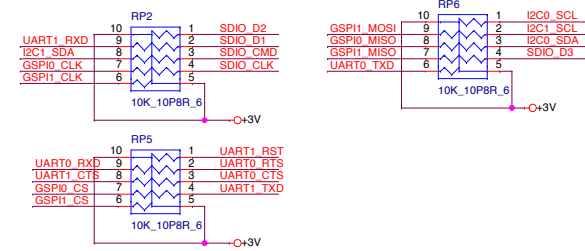
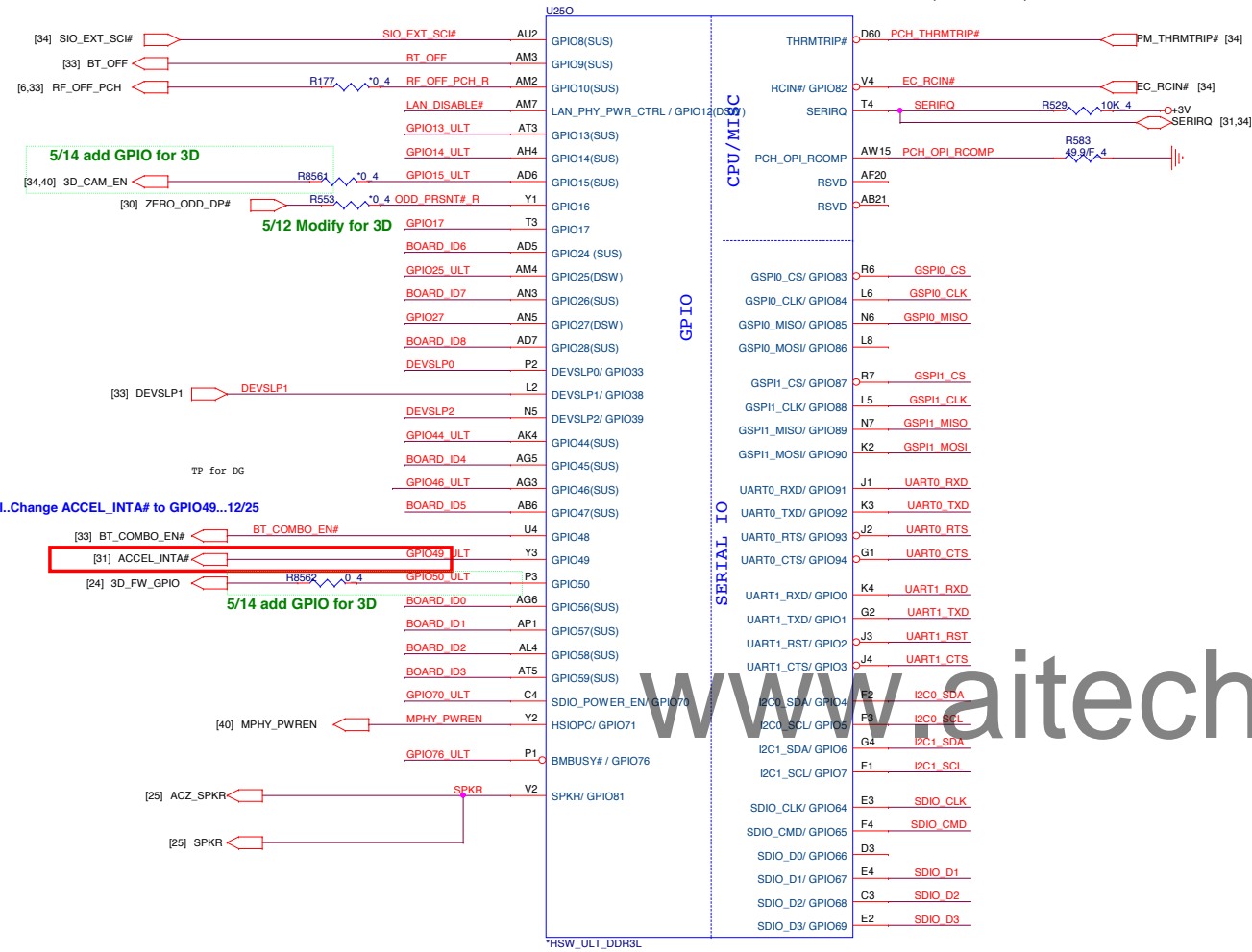


PROJECT : Y11C  
Quanta Computer Inc.

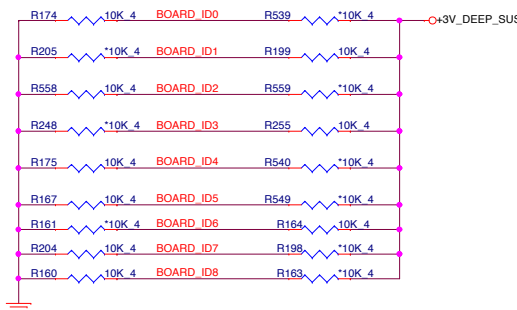
Size	Document Number	Rev
Custom	ULT 7/9 (PCIE/USB/CLK)	1A
Date: Tuesday, September 02, 2014	Sheet 8 of 44	

Lynx Point-LP Platform Controller Hub  
(HDA,JTAG,SATA) Haswell (GPIO)

09



Model	BOARD_ID[6-5] 10 3D Camera	BOARD_ID4 Reserve	BOARD_ID3 0 Pavillian 1 Envy	BOARD_ID[2-1] 00 14" 01 15" 10 17"	BOARD_ID0 0 : UMA 1 : DIS



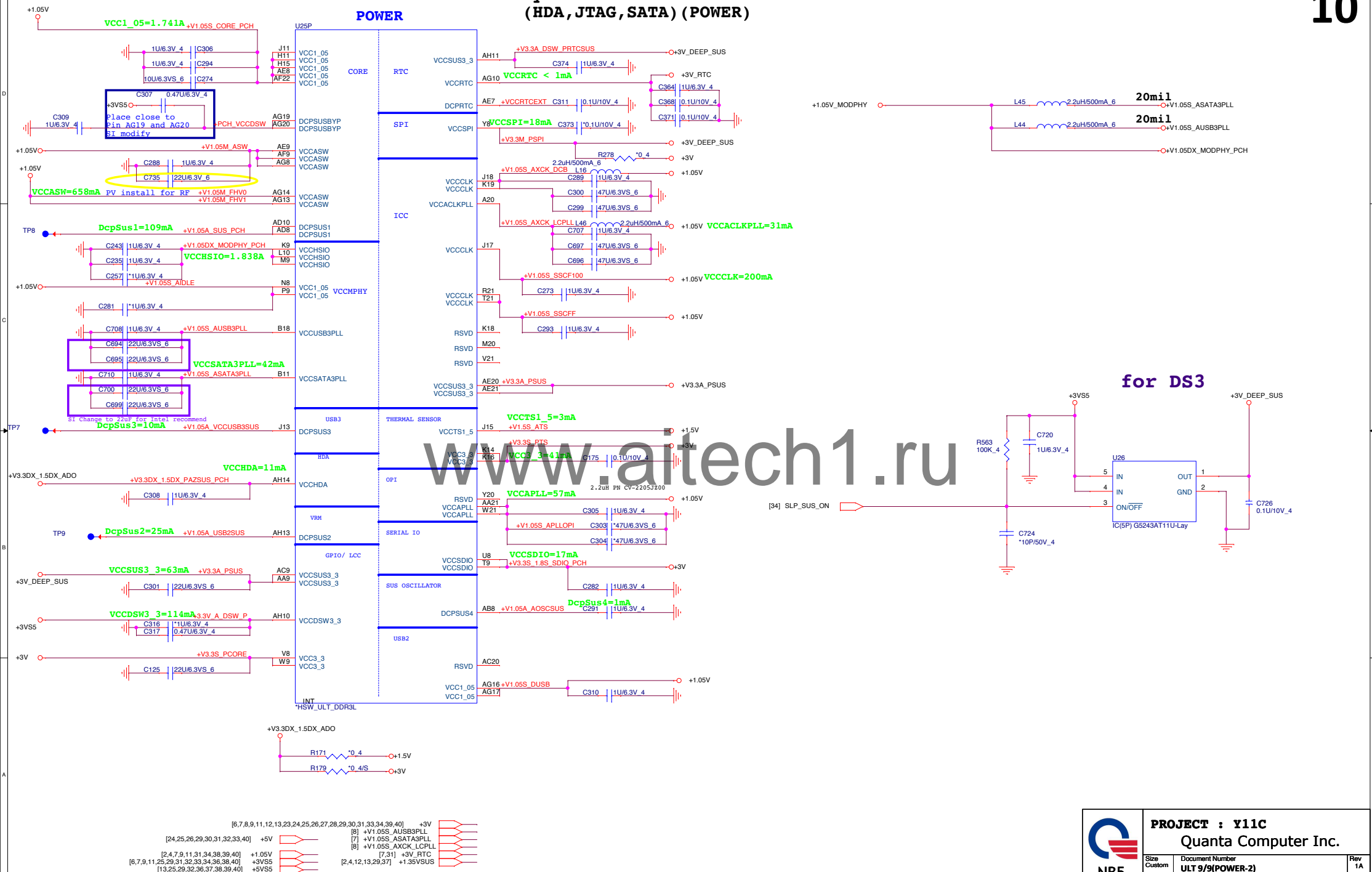
	DIS	UMA
Stuff	Ra	Rb
NC	Rb	Ra

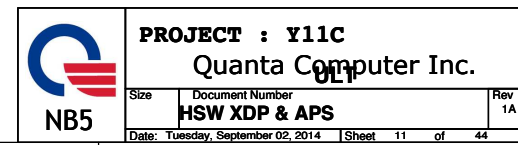
**PROJECT : Y11C**  
**Quanta Computer Inc.**

Size Custom    Document Number **ULT 8/9 (GPIO/MISC)**    Rev 1A

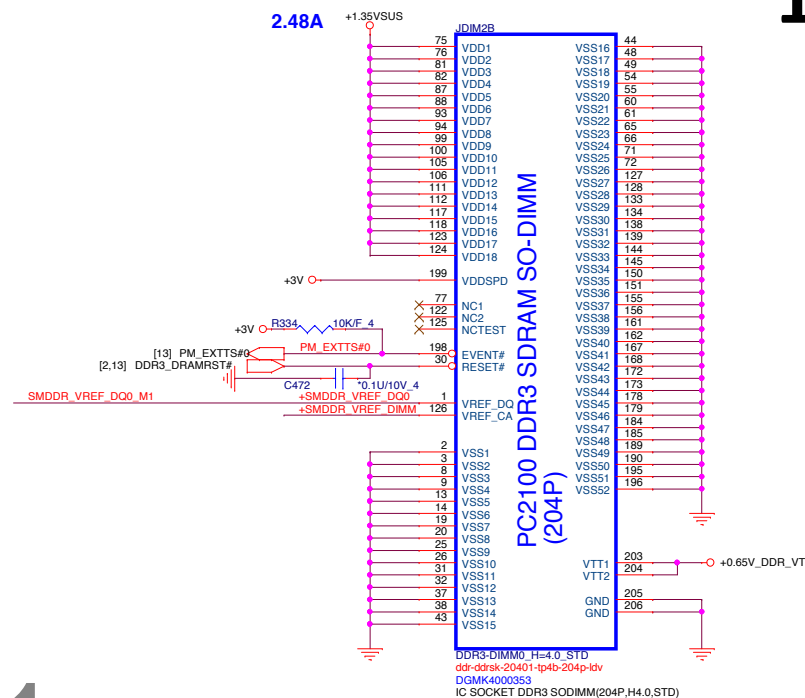
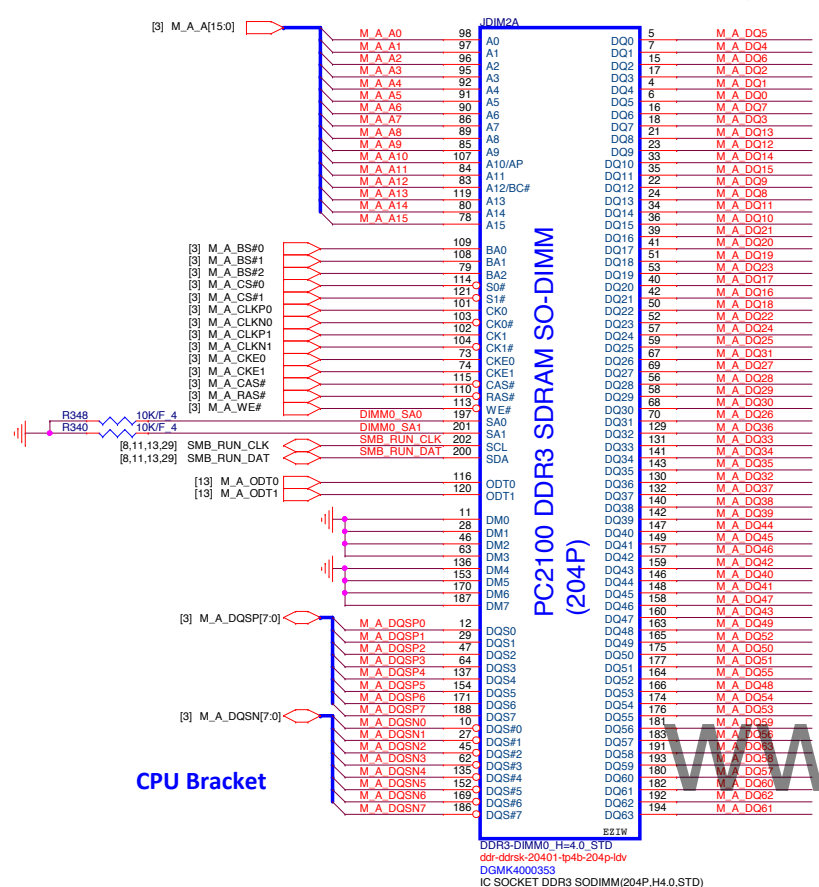
Date: Tuesday, September 02, 2014    Sheet 9 of 44

# Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA) (POWER)



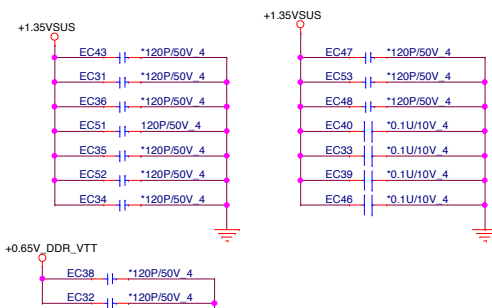






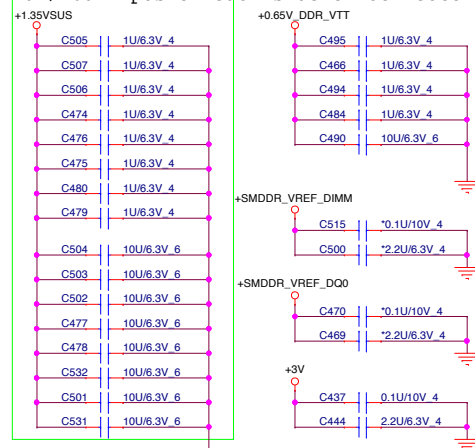
174 M A DQ54  
176 M A DQ53  
181 M A DQ59  
183 M A DQ56  
191 M A DQ83  
193 M A DQ38  
180 M A DQ57  
182 M A DQ60

**For EMI RESERVE**

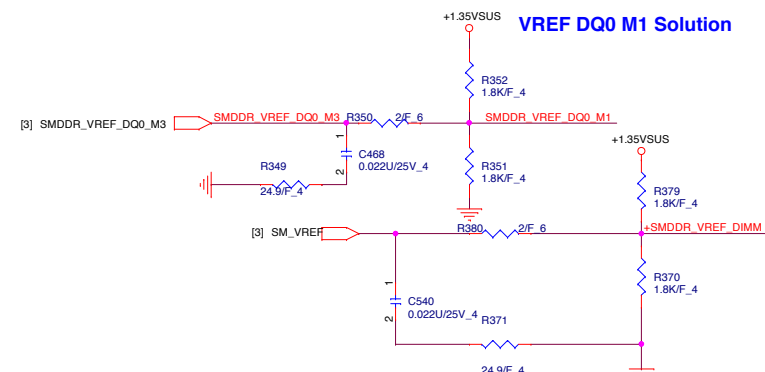


**Place these Caps near So-Dimm0.**

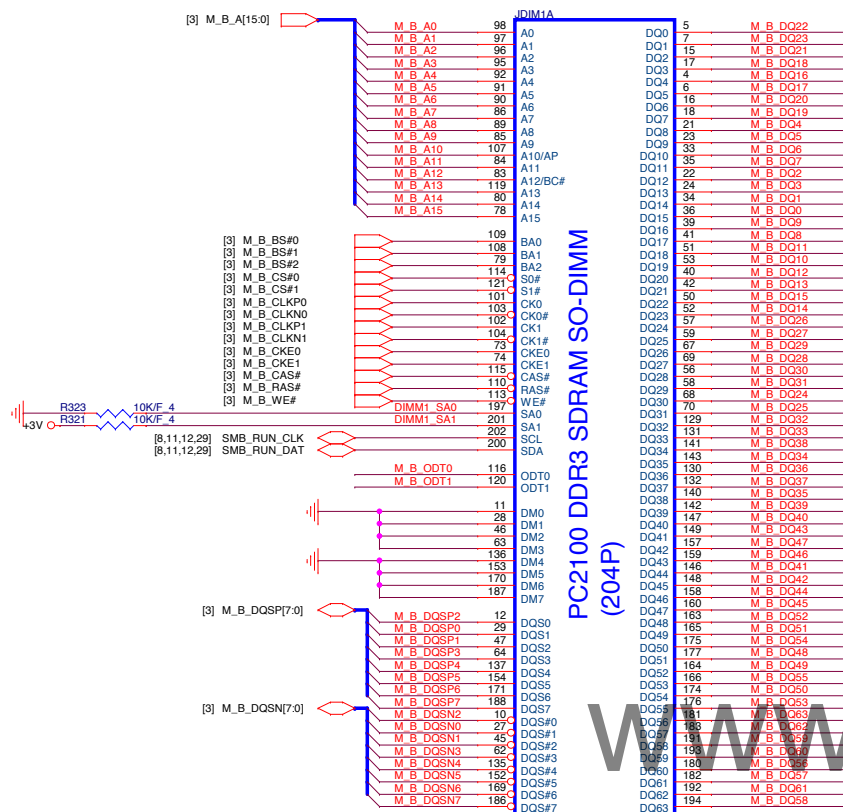
1uF/10uF 4pcs on each side of connector



### VREF DQ0 M1 Solution



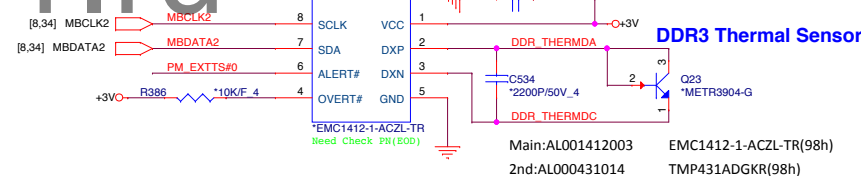
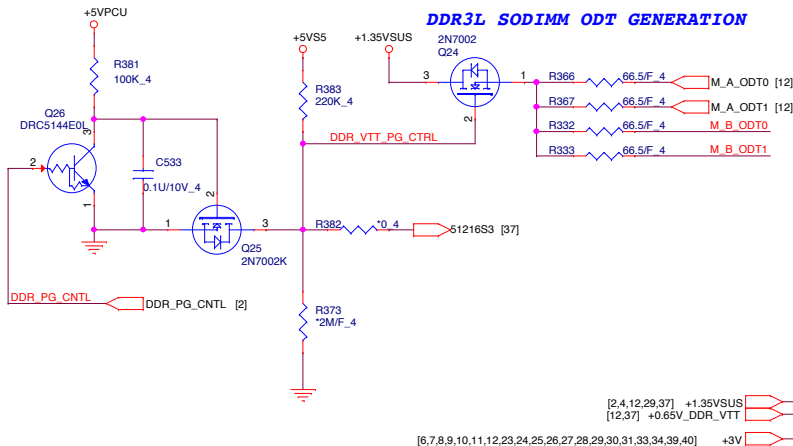




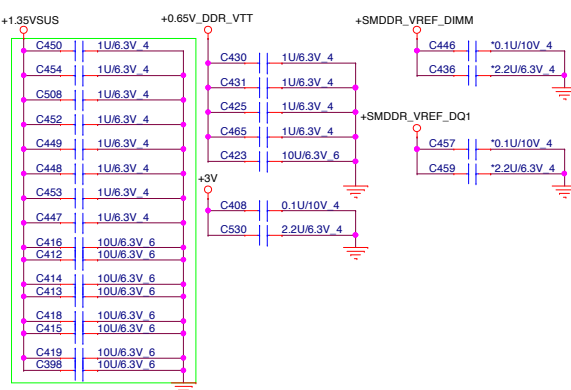
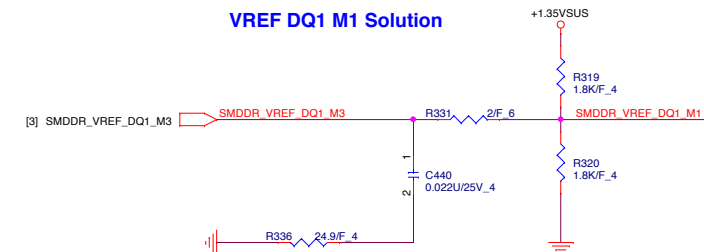
DDR3-DIMM1\_H=4.0\_RVS  
ddr-ddr3k-20401-tp4b-204p-ruv  
DGMK4000264

Local Thermal Sensor

MV可移除

**DDR3L SODIMM ODT GENERATION****Place these Caps near So-Dimm1.**


1uF/10uF 4pcs on each side of connector

**VREF DQ1 M1 Solution**


**PROJECT : Y11C**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	DDR3 DIMM1-RV5(4.0H)	1A
Date: Tuesday, September 02, 2014	Sheet	44


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		<b>PROJECT :Y05</b> Quanta Computer Inc.	
		Size Custom	Document Number <b>N15S-GT (PCIE VF) /NVDD</b>
		Date: Tuesday, September 02, 2014	Sheet 14 of 44


[www.aitech1.ru](http://www.aitech1.ru)

		<b>PROJECT :Y05</b> Quanta Computer Inc.			
Size Custom	Document Number <b>N15S-GT (MEMORY/GND)</b>				Rev 2A
Date: Tuesday, September 02, 2014   Sheet 15 of 44					


[www.aitech1.ru](http://www.aitech1.ru)

	<b>PROJECT :Y05</b> Quanta Computer Inc.				
	Size Custom	Document Number <b>N15S-GT (DISPLAY)</b>			Rev 2A
	Date: Tuesday, September 02, 2014   Sheet 16 of 44				


[www.aitech1.ru](http://www.aitech1.ru)

		<b>PROJECT :Y05</b> Quanta Computer Inc.	
		Size Custom	Document Number <b>N15S-GT (GPIO/STRAPS)</b>
Date: Tuesday, September 02, 2014		Sheet 17	Rev 2A
		of 44	


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		<b>PROJECT :U82</b> Quanta Computer Inc.			
Size Custom	Document Number <b>N14M-GS (PCIE VF) /NVDD</b>				Rev 2A
Date: Tuesday, September 02, 2014		Sheet 18		of 44	

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		<b>PROJECT :U82</b> Quanta Computer Inc.		
Size Custom	Document Number <b>N14M-GS (MEMORY/GND)</b>			Rev 2A
Date: Tuesday, September 02, 2014		Sheet 19 of 44		

[www.aitech1.ru](http://www.aitech1.ru)


			<b>PROJECT :U82</b> Quanta Computer Inc.		
Size Custom	Document Number <b>N14M-GS (DISPLAY)</b>				Rev 2A
Date: Tuesday, September 02, 2014			Sheet	20	of 44



[www.aitech1.ru](http://www.aitech1.ru)

	<b>PROJECT :U82</b> Quanta Computer Inc.				
	Size Custom	Document Number <b>N14M-GS (GPIO/STRAPS)</b>			Rev 2A
	Date: Tuesday, September 02, 2014   Sheet 21 of 44				

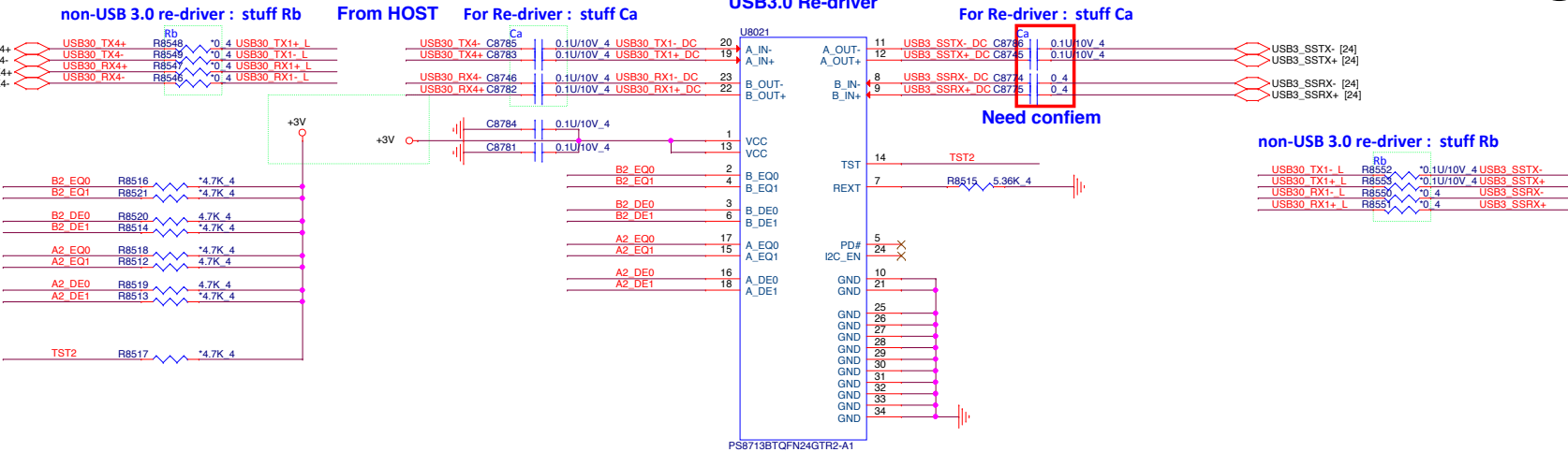
www.aitech1.ru

	<b>PROJECT :U82</b> Quanta Computer Inc.				
	Size Custom	Document Number <b>DGPU Memory (DDR3)</b>			Rev 2A
	Date: Tuesday, September 02, 2014   Sheet 22 of 44				

AEQ 9.5db / ADE 3.5db  
BEQ 13db / BDE 5db / REXT 5.36K

A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5db	0	0	3.5db
0	1	13db	0	1	no de-emphasis
1	0	4.5db	1	0	2.7db
1	1	7.5db	1	1	5db

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing



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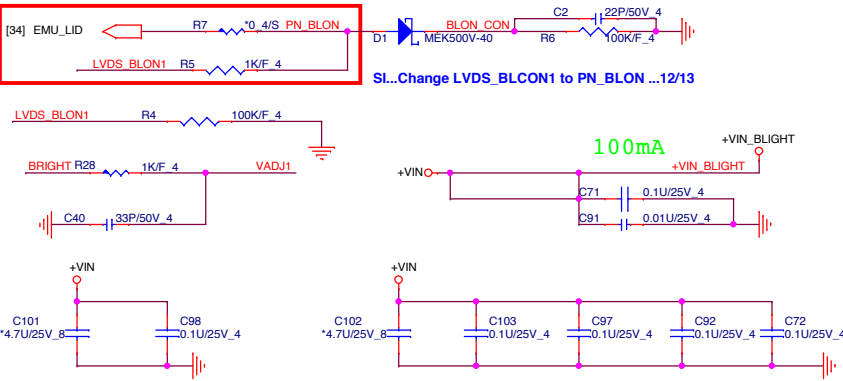
PROJECT : Y11C  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTD2136	1A
Date: Tuesday, September 02, 2014   Sheet 23 of 44		

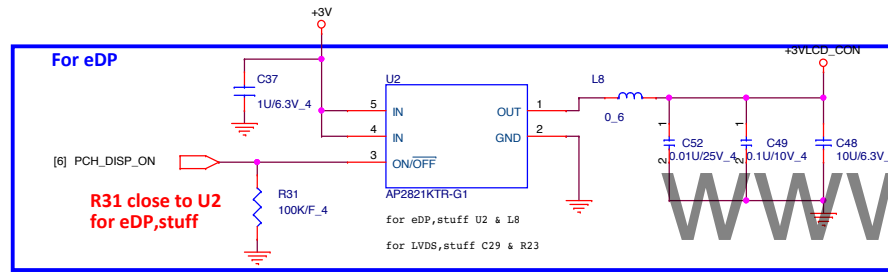
# LID Switch

LVDS Conn.

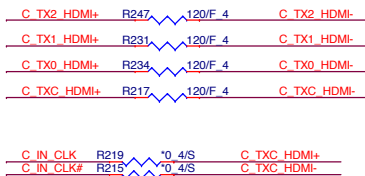
24



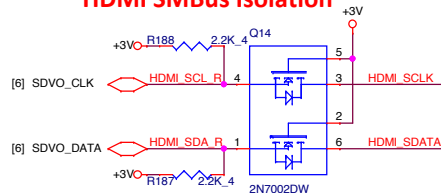
5/12 Modify for 3D



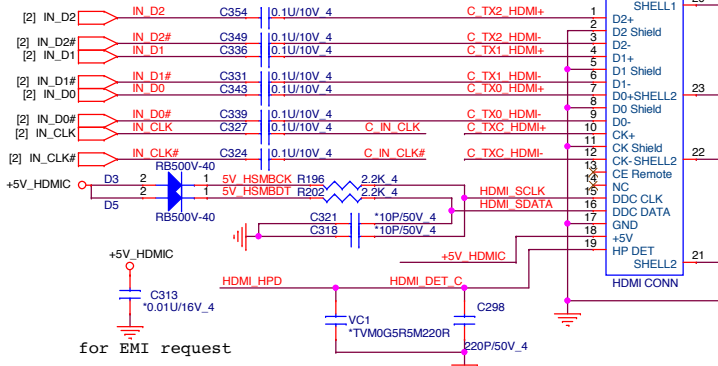
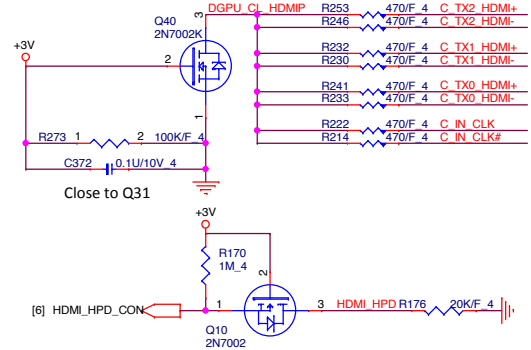
## EMI Solution



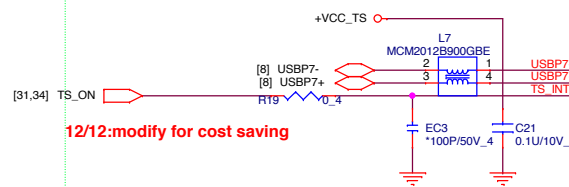
## HDMI SMBus Isolation



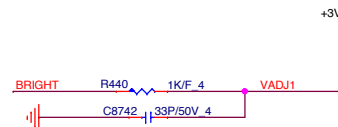
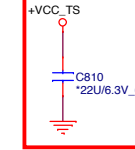
## Close to HDMI connector



5/12 Modify for 3D

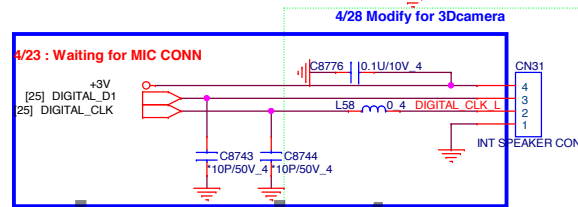


MV..Add 22u at +VCC\_TS for RF...3/28



8/21 PV Stuff C12 for EMI

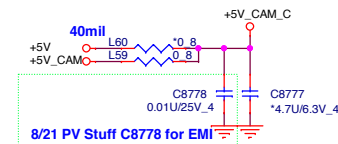
4/24 Modify for 3Dcamera



5/12 Add for 3D Camera



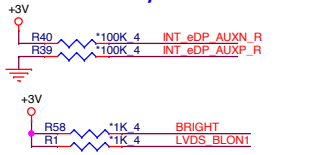
5/12 Add 3D Camera power



For EDP Only: stuff Rd,Re,Rf



For EDP Only: stuff



**PROJECT : Y11C**

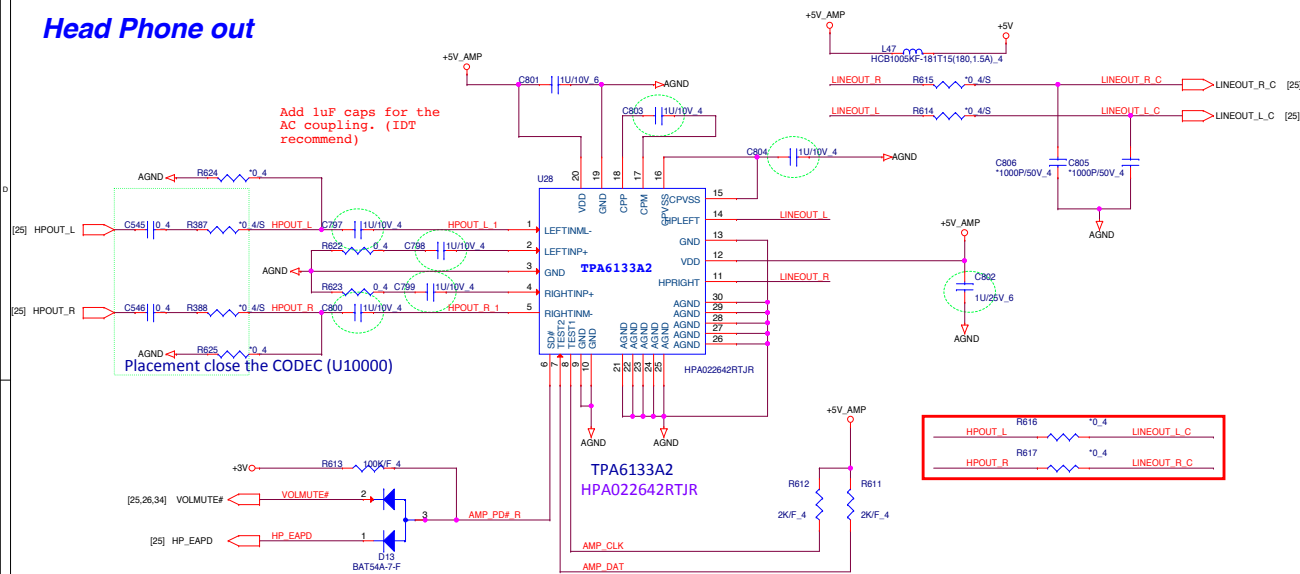
**Quanta Computer Inc.**

Size	Document Number	Rev	1A
Custom	LCD CONN/LID/CAM/D-MIC		

Date: Tuesday, September 02, 2014 Sheet 24 of 44

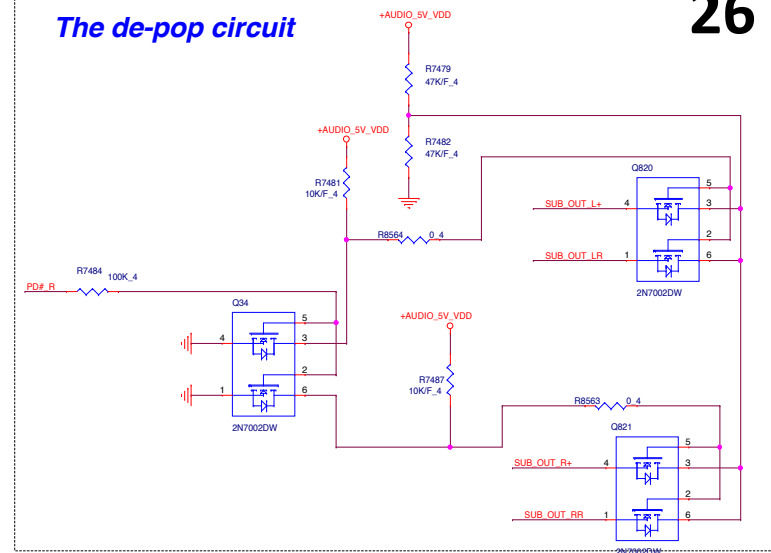


## Head Phone out

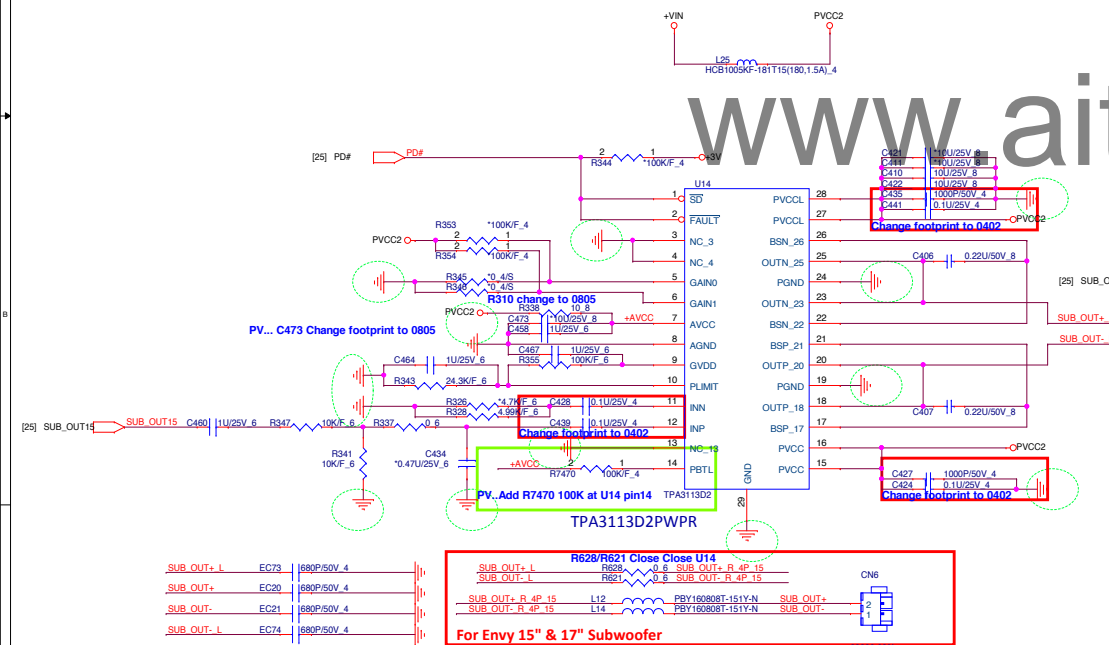


### *The de-pop circuit*

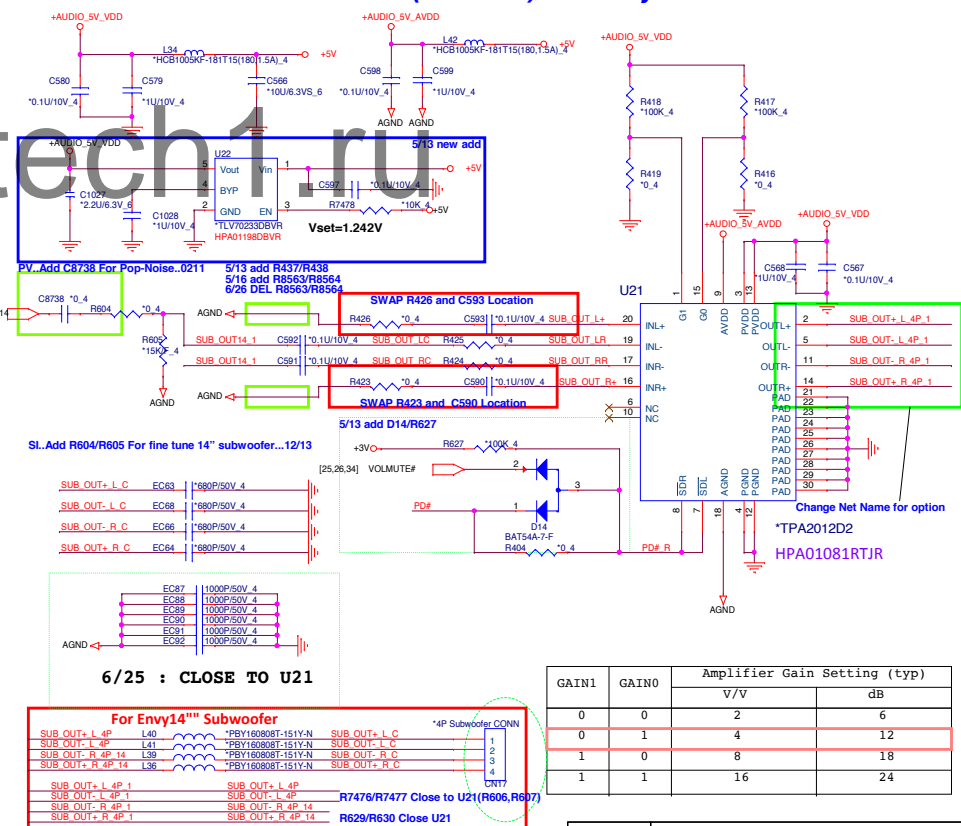
26



***For Envy 15" & 17" Subwoofer***

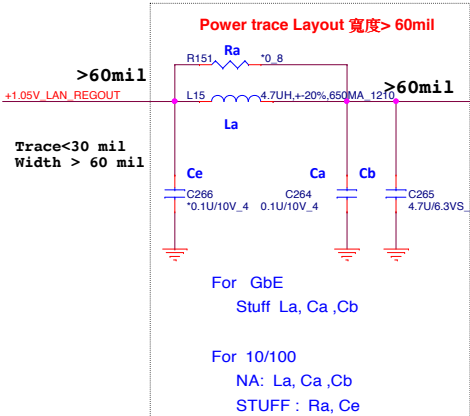
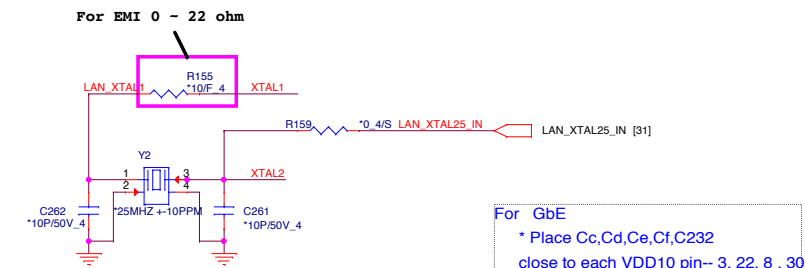


**For Pavilion 15" Subwoofer(Reserve)For Envy14"" Subwoofer**



GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

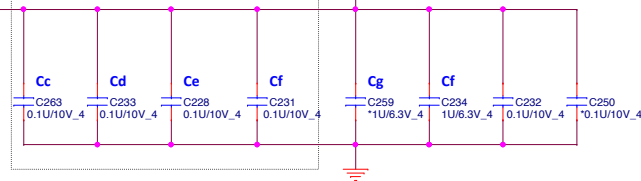
GAIN1	GAIN0	Amplifier Gain Setting (typ)	
		V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24



For GbE

- \* Place Cc,Cd,Ce,Cf,C232 close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf  
\* Place Ce , Cf ,C250  
close to each VDD10 pin-- 8, 30 only,



For GbE

- \* Place Cf close to each VDD10 pin-- 22 (reserve)

For 10/100

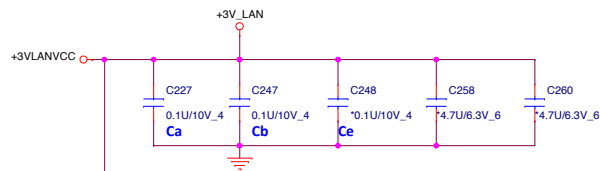
\* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100

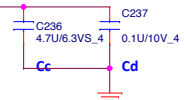
- \* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA

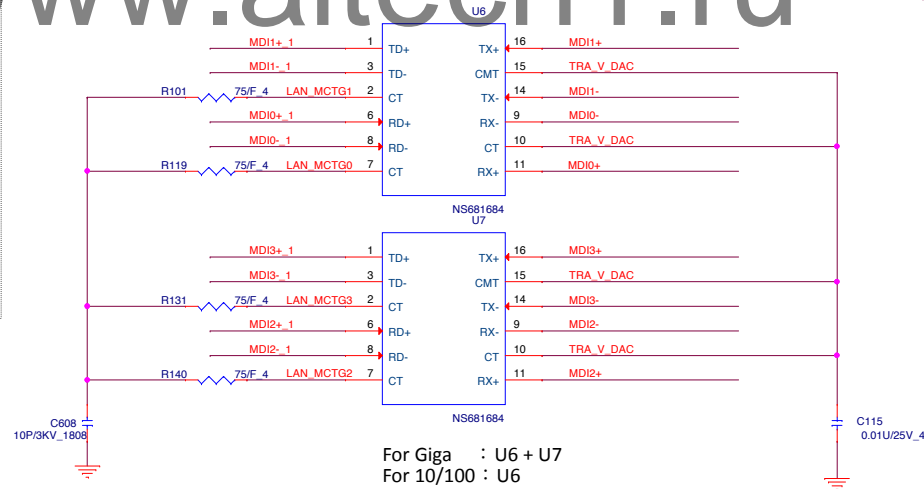
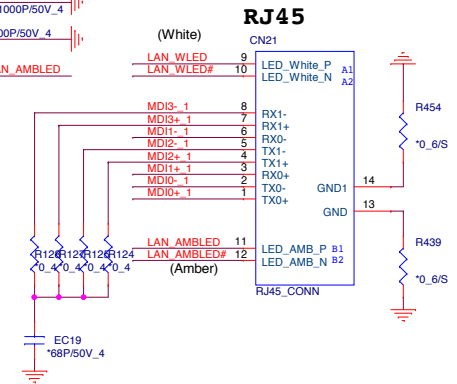
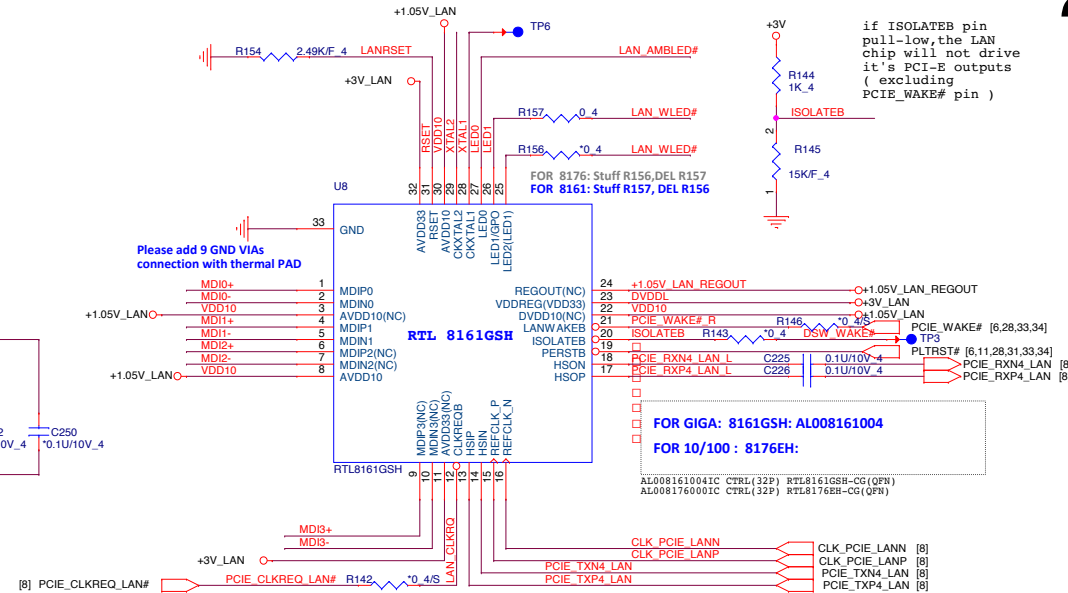
- \* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



\* Place Cc and Cd close to each VDD33 pin-- 23

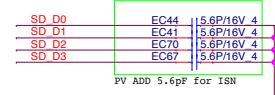


For 10/100  
NA: Cc, Cd



For Giga :  $U_6 + U_7$   
For 10/100 :  $U_6$

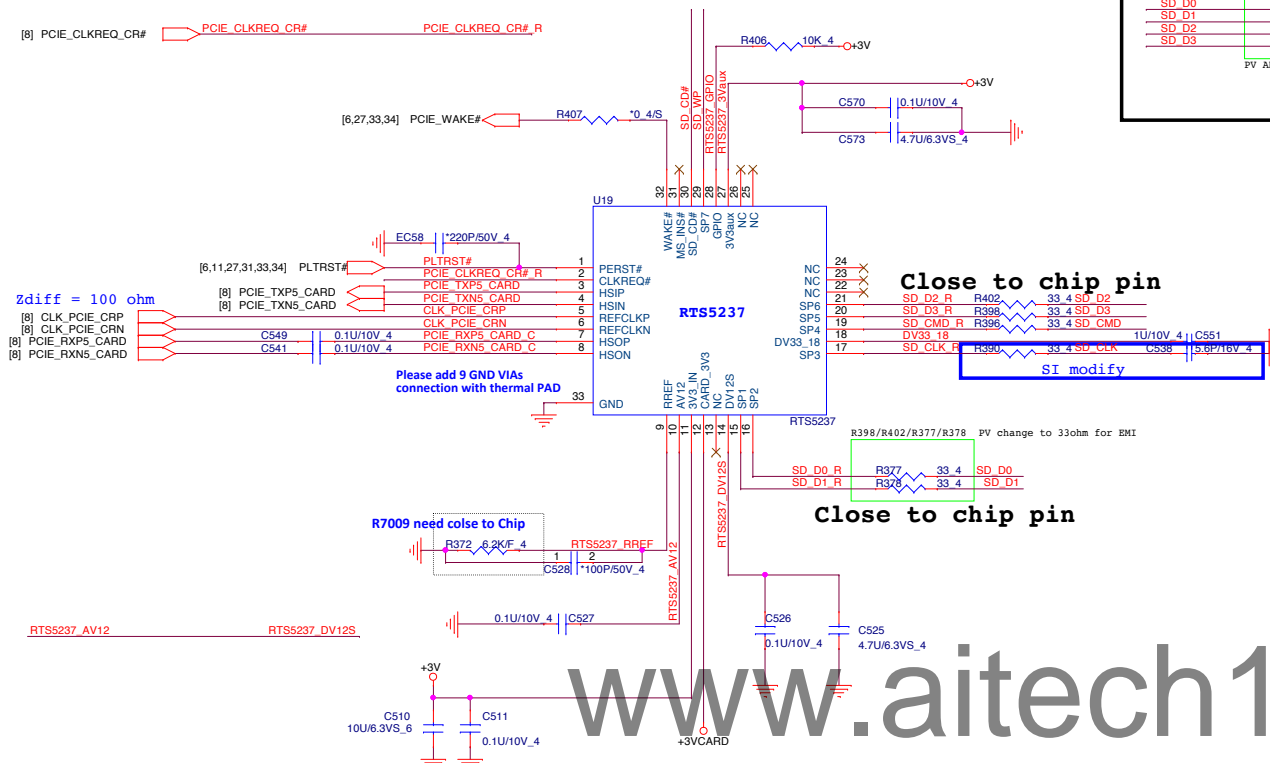
Reserve for EMI



SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

## Share Pin

SD / MMC



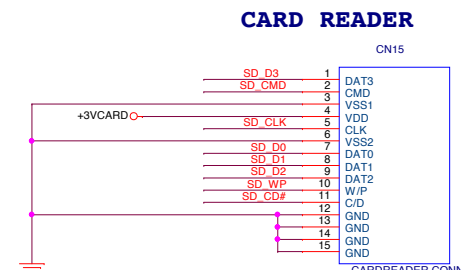
NC 24 ✗  
NC 23 ✗  
NC 22 ✗

**Close to chip pin**

SI modify

Close to chip pin

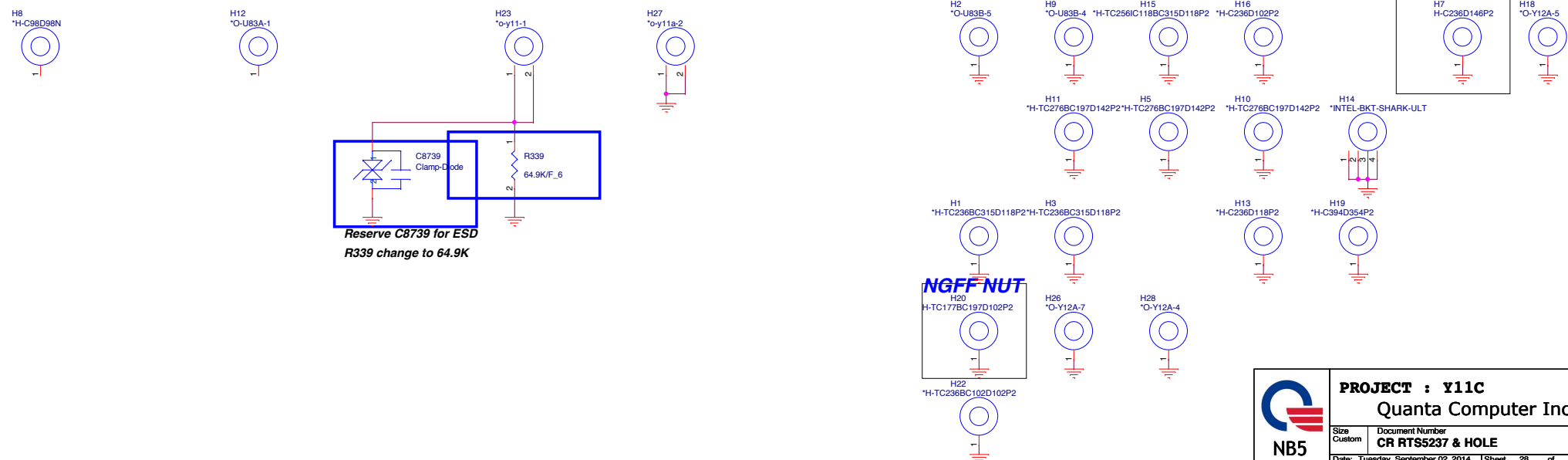
CLOSE CONN



**CARD READER**

## R6x Type

## Thermal Nut

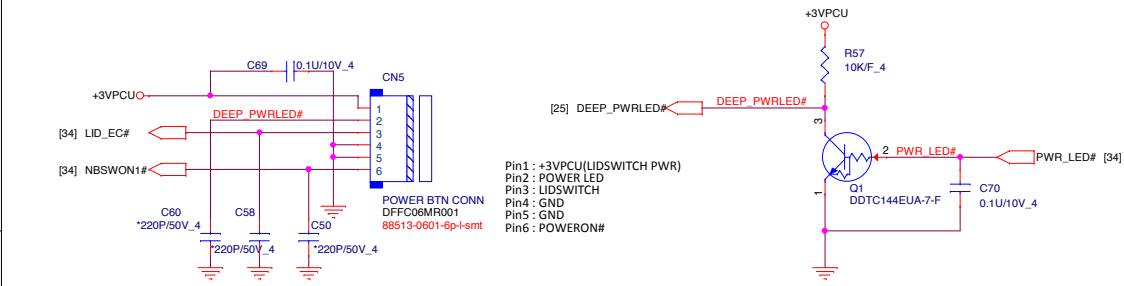


**Reserve C8739 for ESD**  
**R339 change to 64.9K**

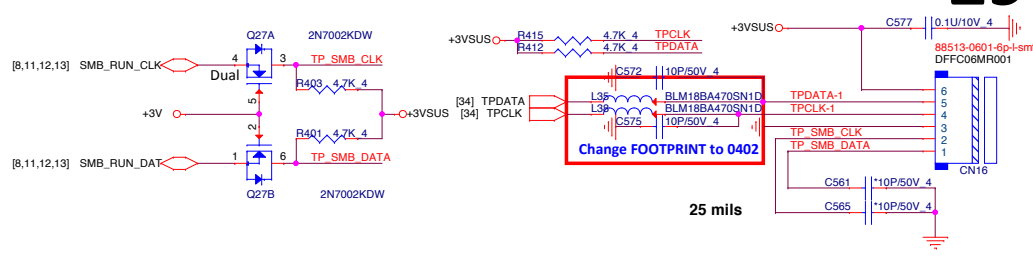
**NGFF NUT**



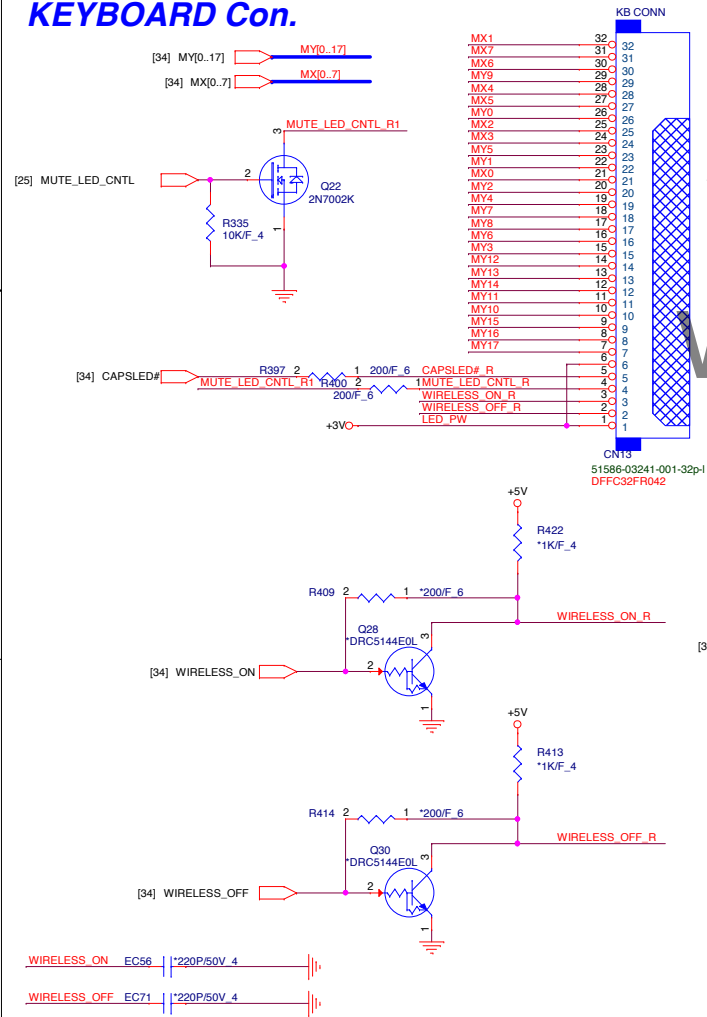
## Power Botton Connector



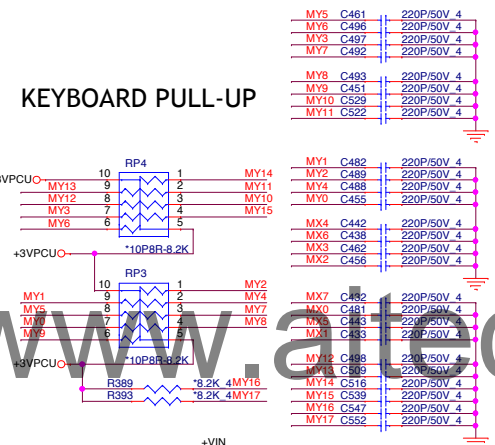
### Touch Pad Connector



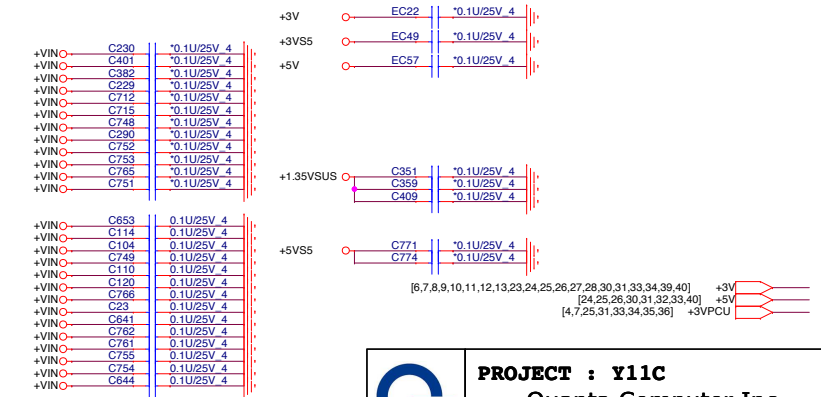
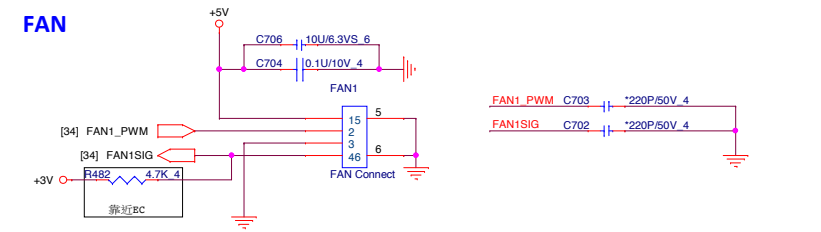
## KEYBOARD Con.



## KEYBOARD PULL-UP

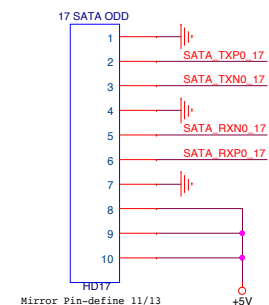
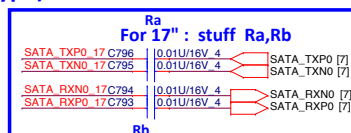


**FAN**

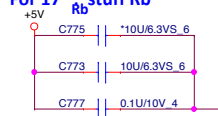


## HDD

## SATA HDD Connector(Cable type) 15.6"

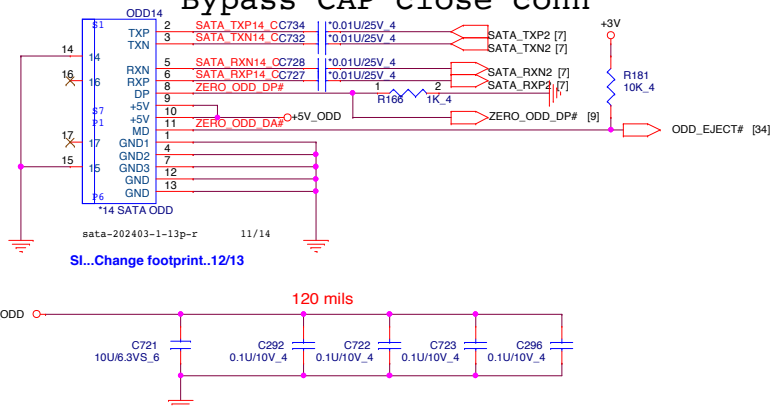


For 17" : stuff Rb

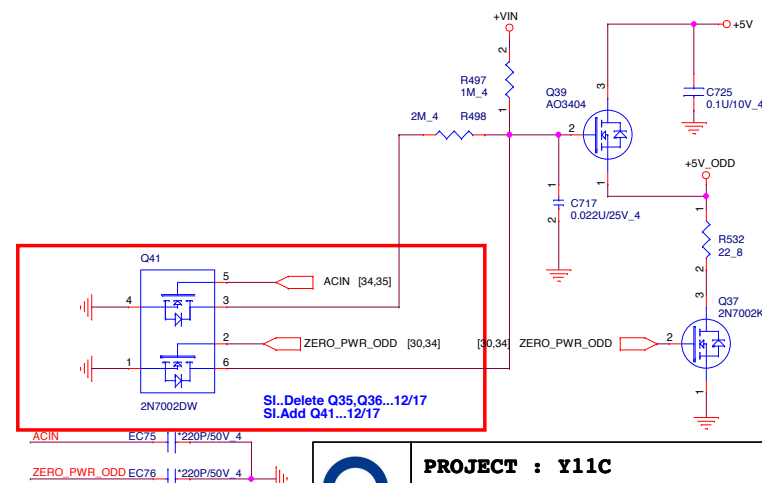
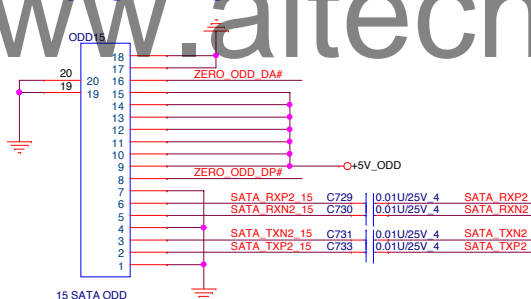
SATA ODD  
CONNECTOR

## 14" SATA ODD

Bypass CAP close conn



## 15" SATA ODD

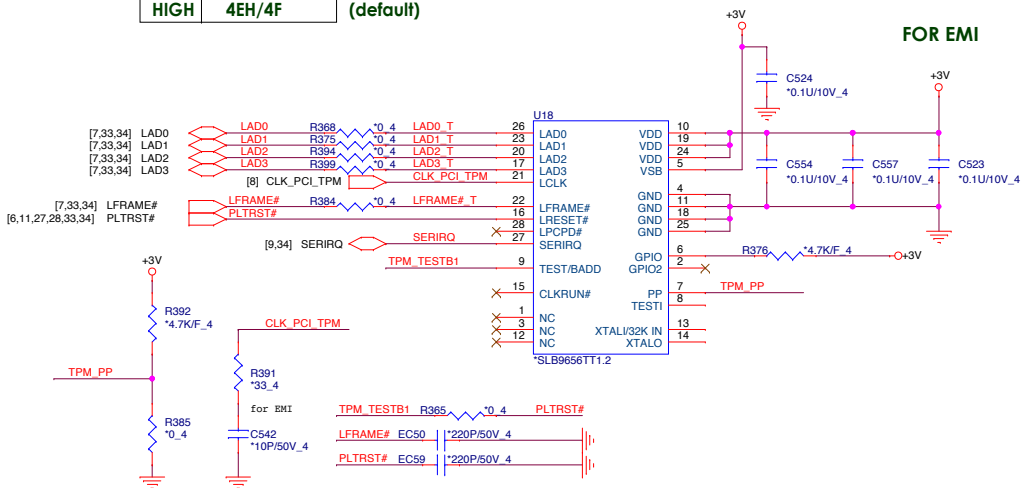
High : ODD power down  
Low : ODD power onPROJECT : Y11C  
Quanta Computer Inc.

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## TPM (1.2)

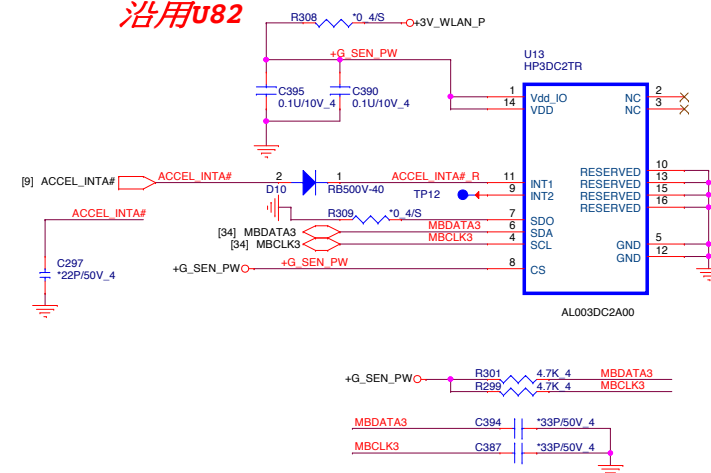
Address

	BADD
HIGH	4EH/4F (default)

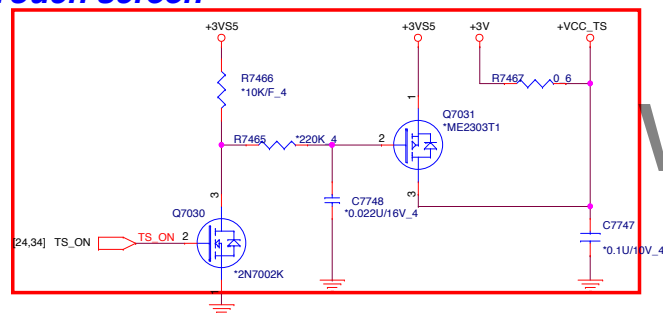


## Accelerometer Sensor

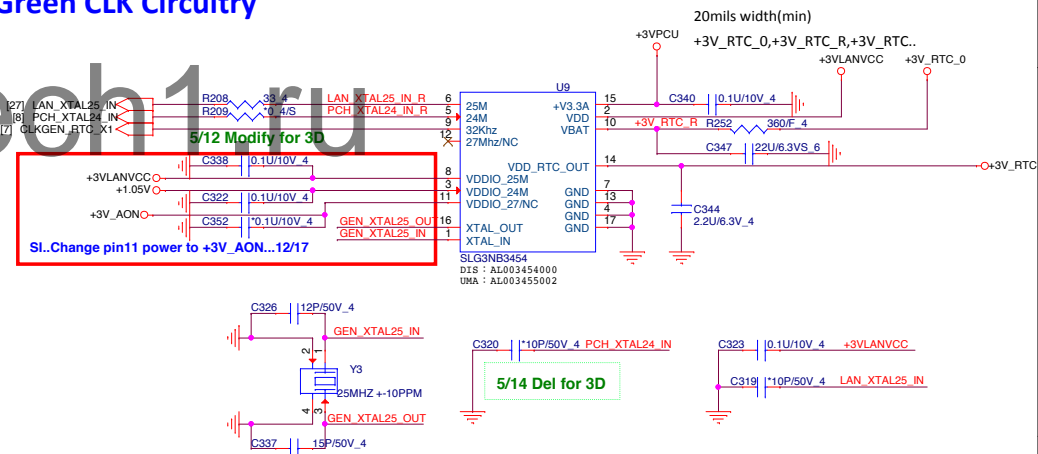
沿用u82



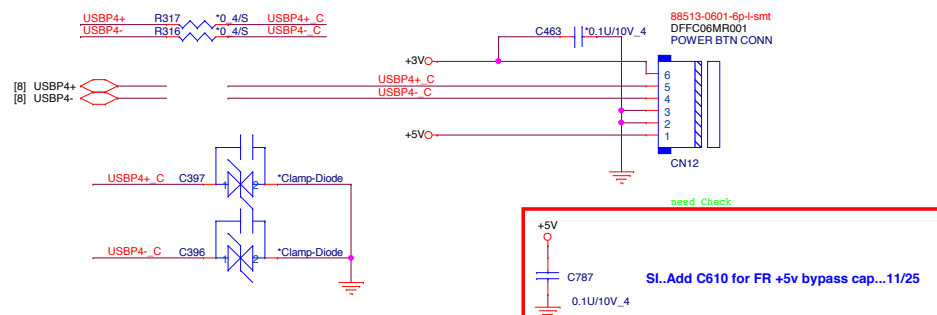
## Touch screen



## Green CLK Circuitry



## Fingerprint Conn

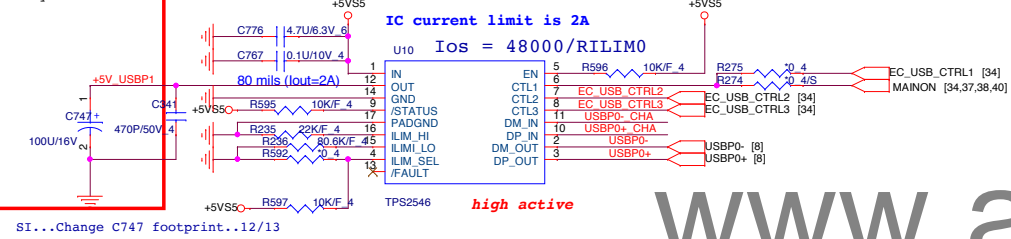


if Envy SKU,non-staff



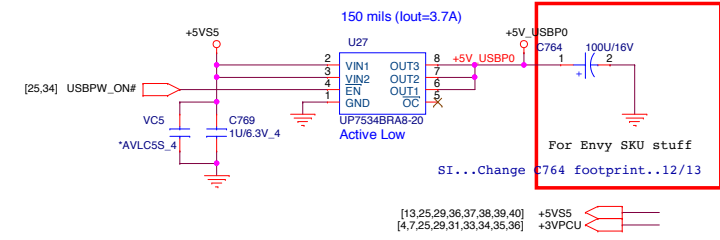
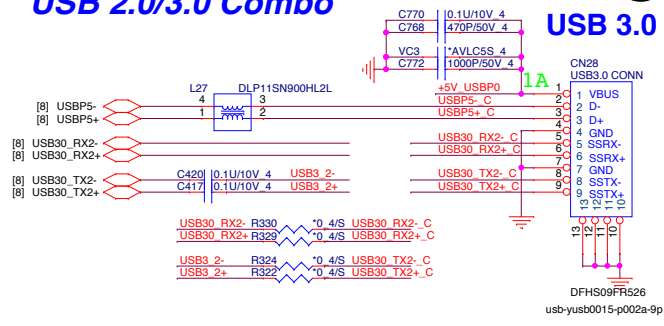
For Pavilion / Envy SKU stuff

for Envy SKU stuff



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### USB 2.0/3.0 Combo

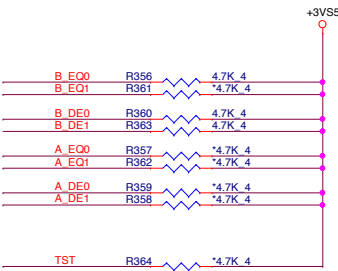


### Right-Side USB3.0 Re-Driver

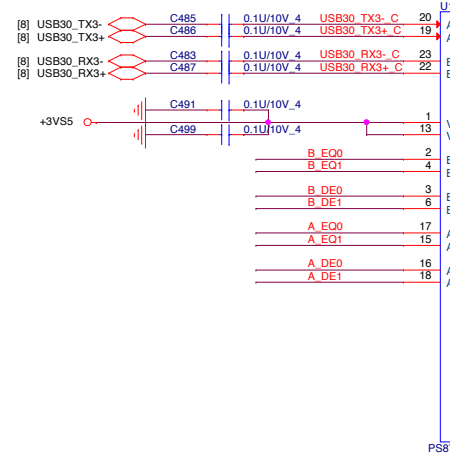
AEQ 9.5db / ADE 3.5db  
BEQ 13db / BDE 5db / REXT 5.36K

A_EQ1	A_EQ0	A_DE1	A_DE0	
B_EQ1	B_EQ0	B_DE1	B_DE0	
0	0	9.5dB	0	3.5dB
0	1	13dB	0	no de-emphasis
1	0	4.5dB	1	2.7dB
1	1	7.5dB	1	5dB

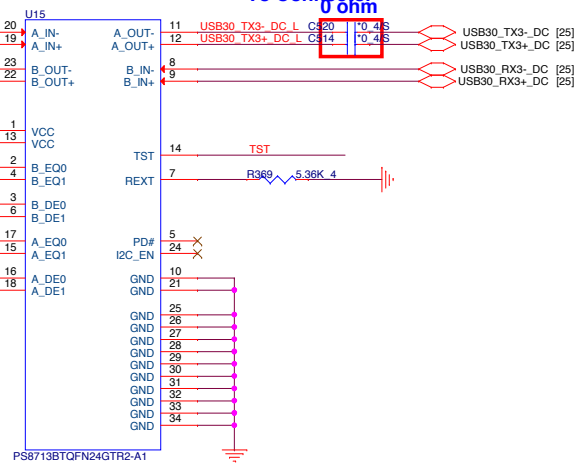
TST : Low = Normal LFPS swing / Right =Turn down LFPS swing



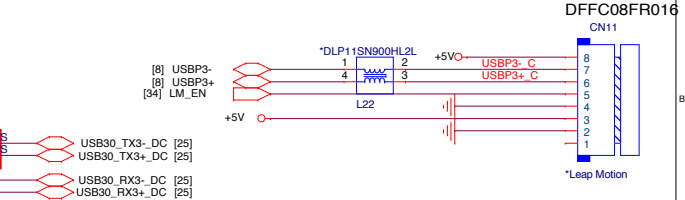
### From HOST

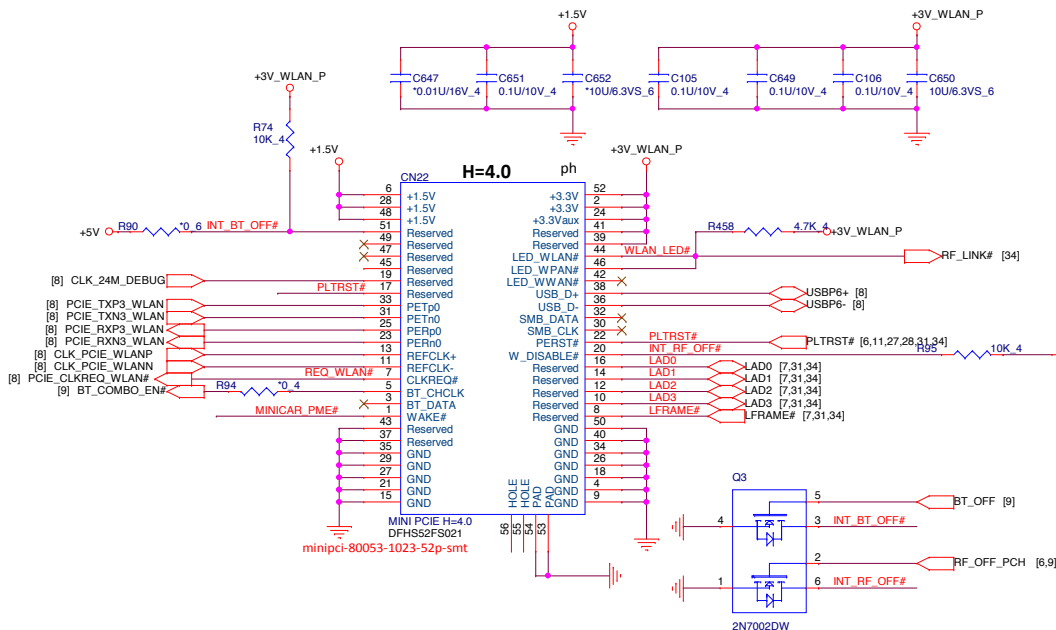


### USB3.0 Re-driver

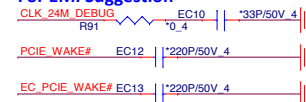


### To Connector

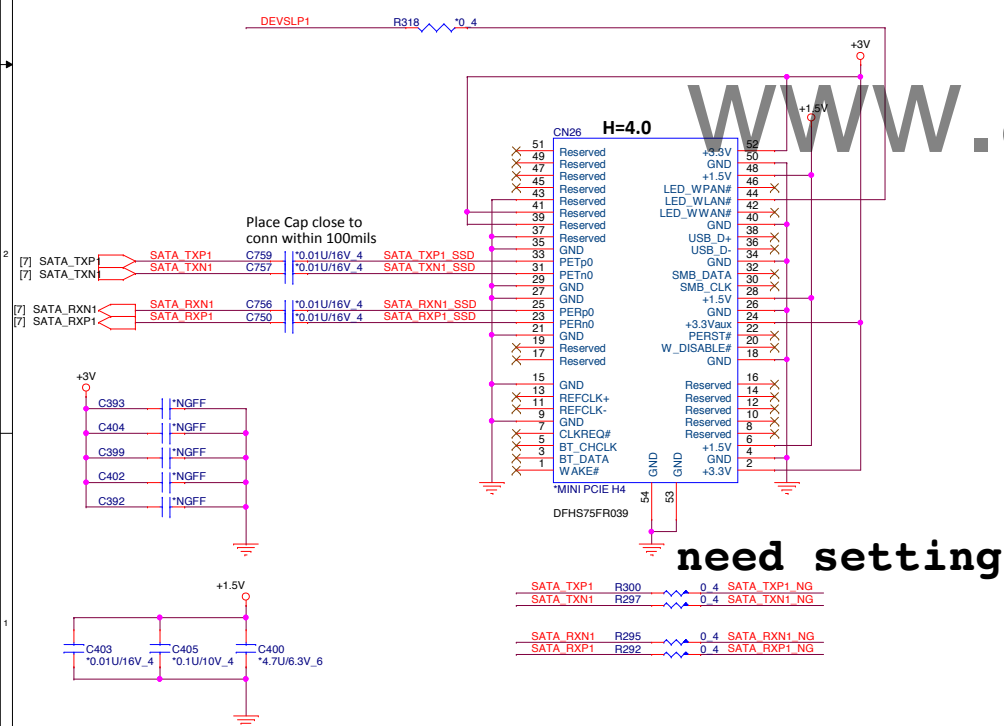
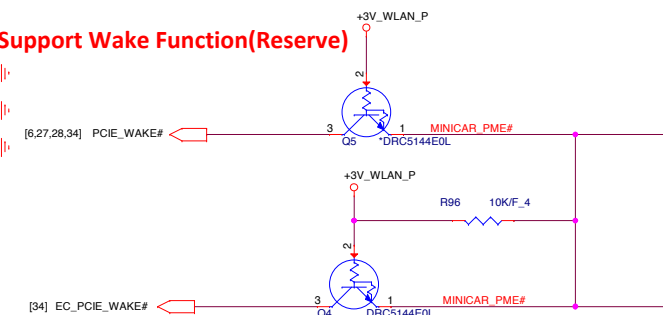




## For EMI Suggestion

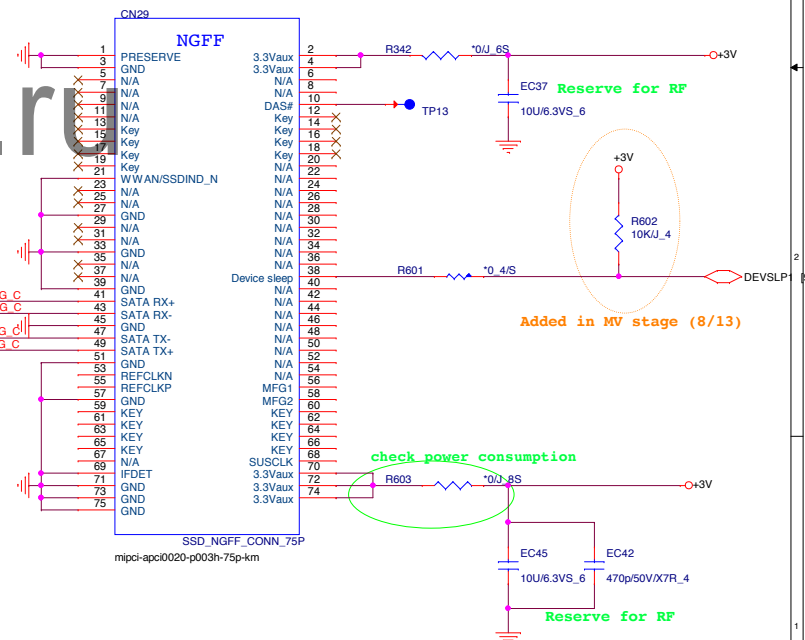
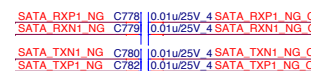


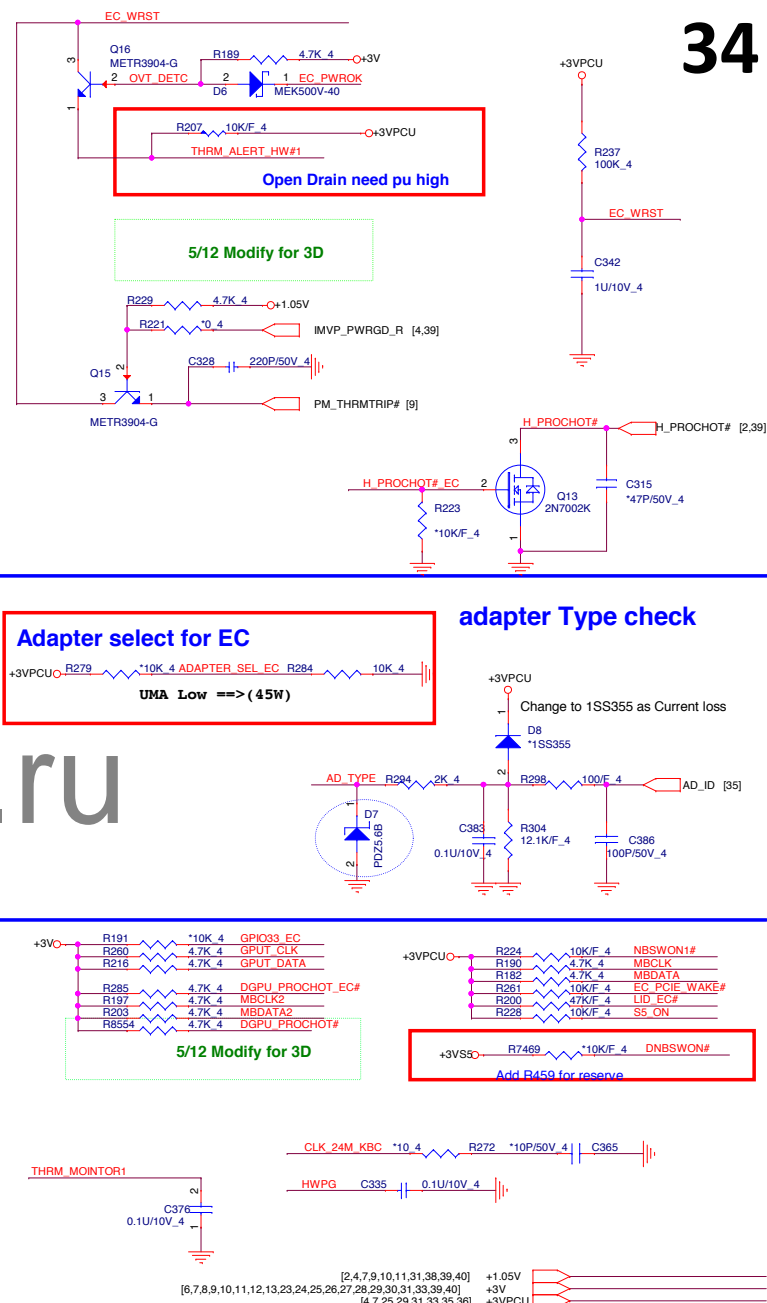
## Support Wake Function(Reserve)



## NGFF-SSD

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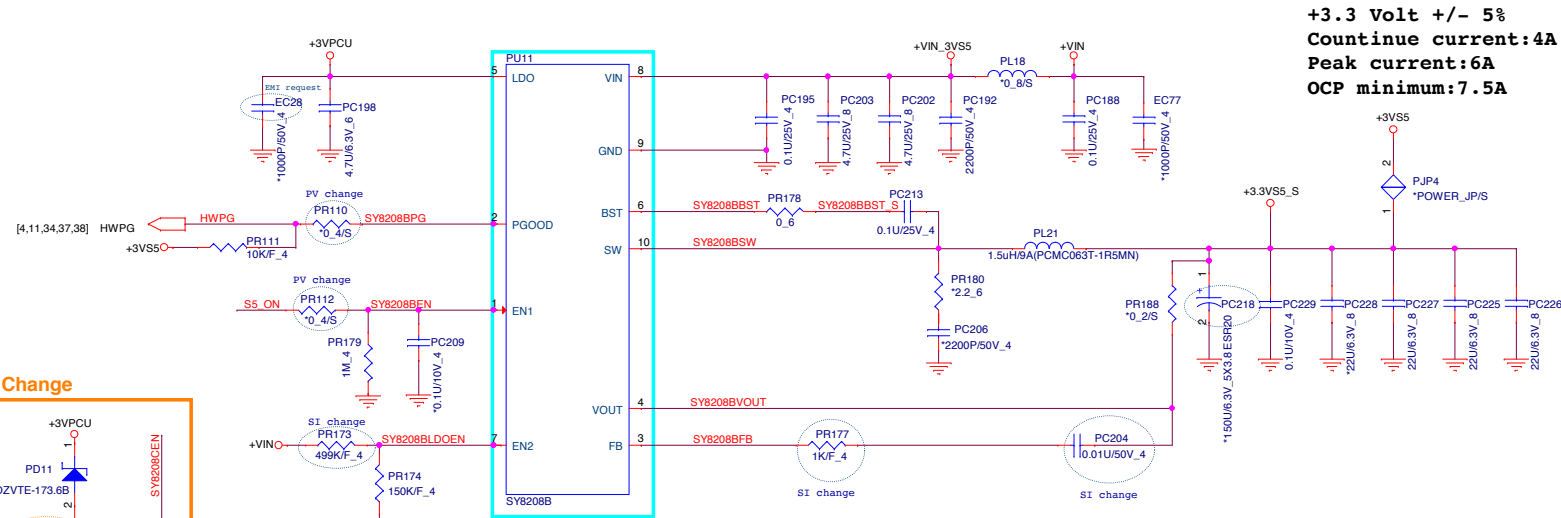




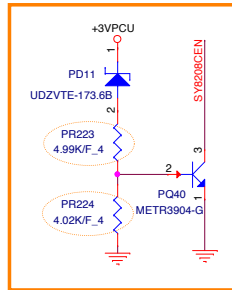




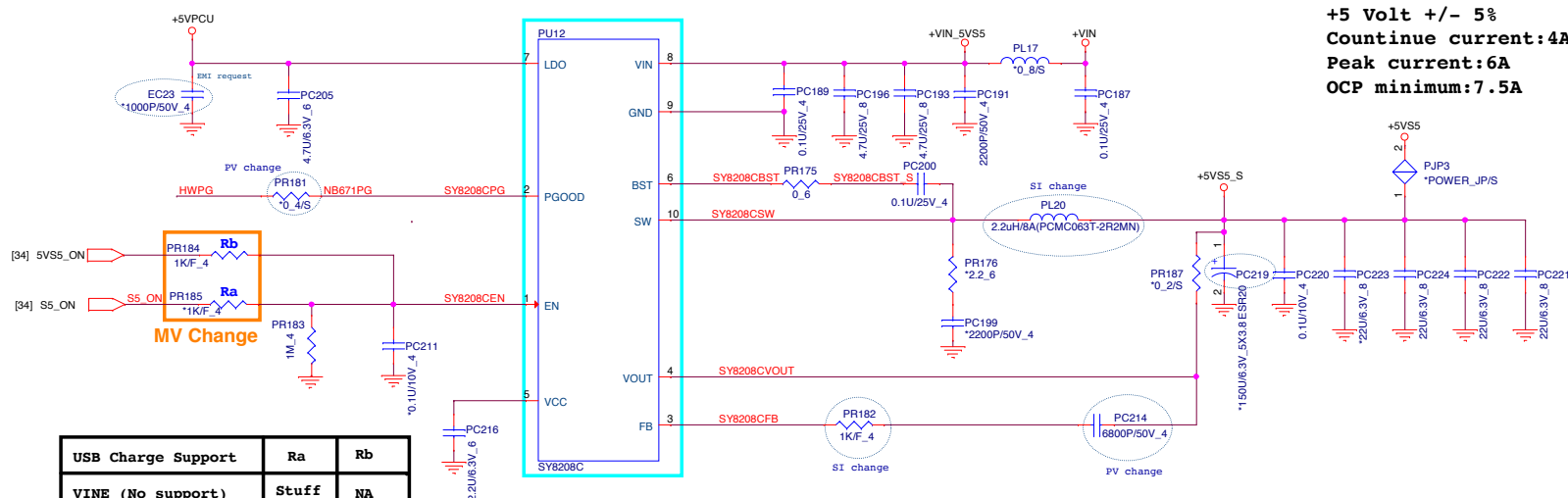
## DC/DC +3VS5/+5VS5



## MV Change

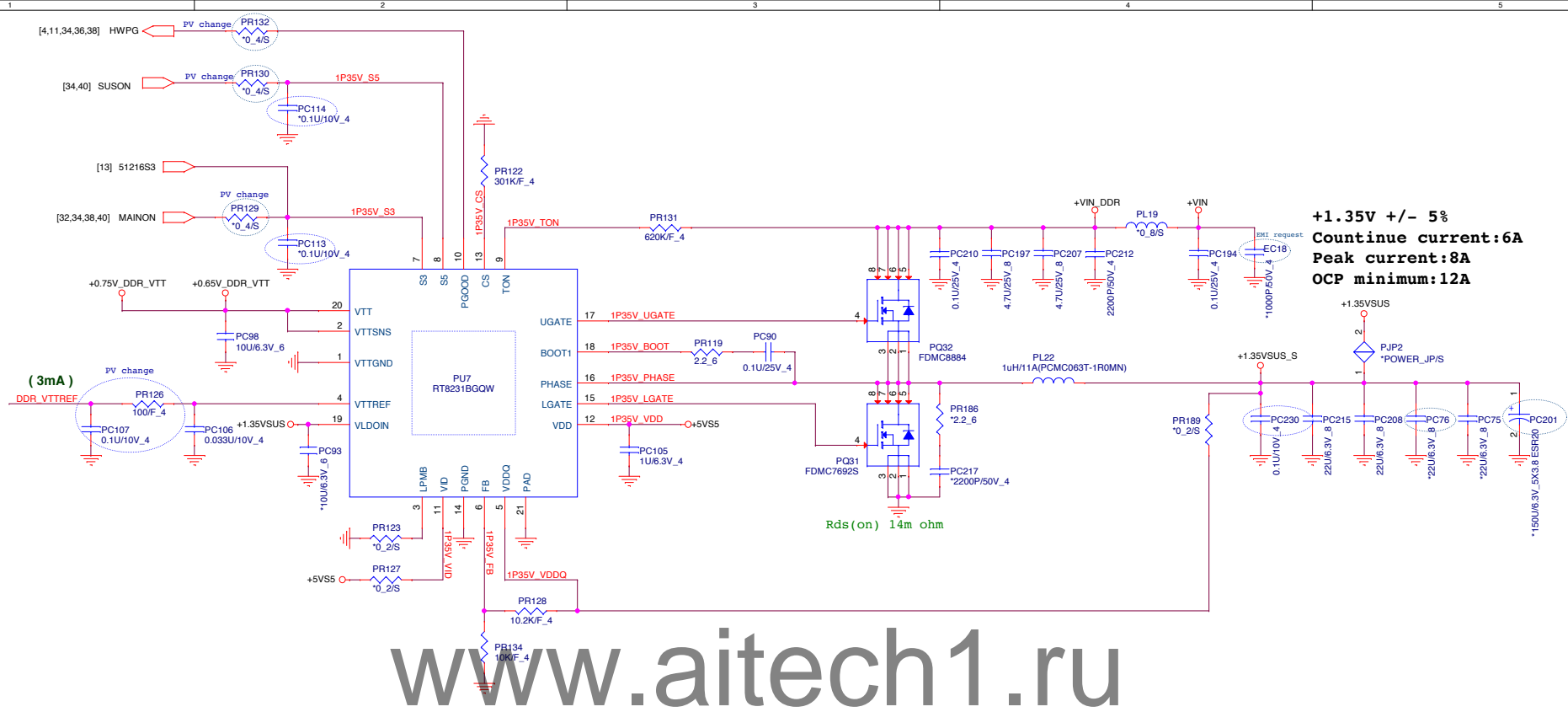


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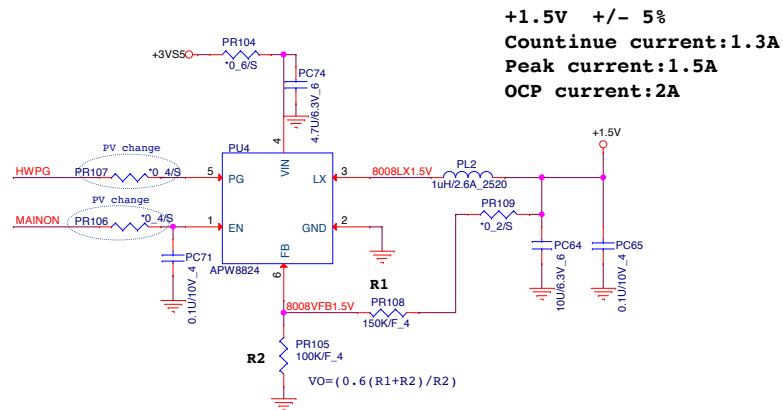
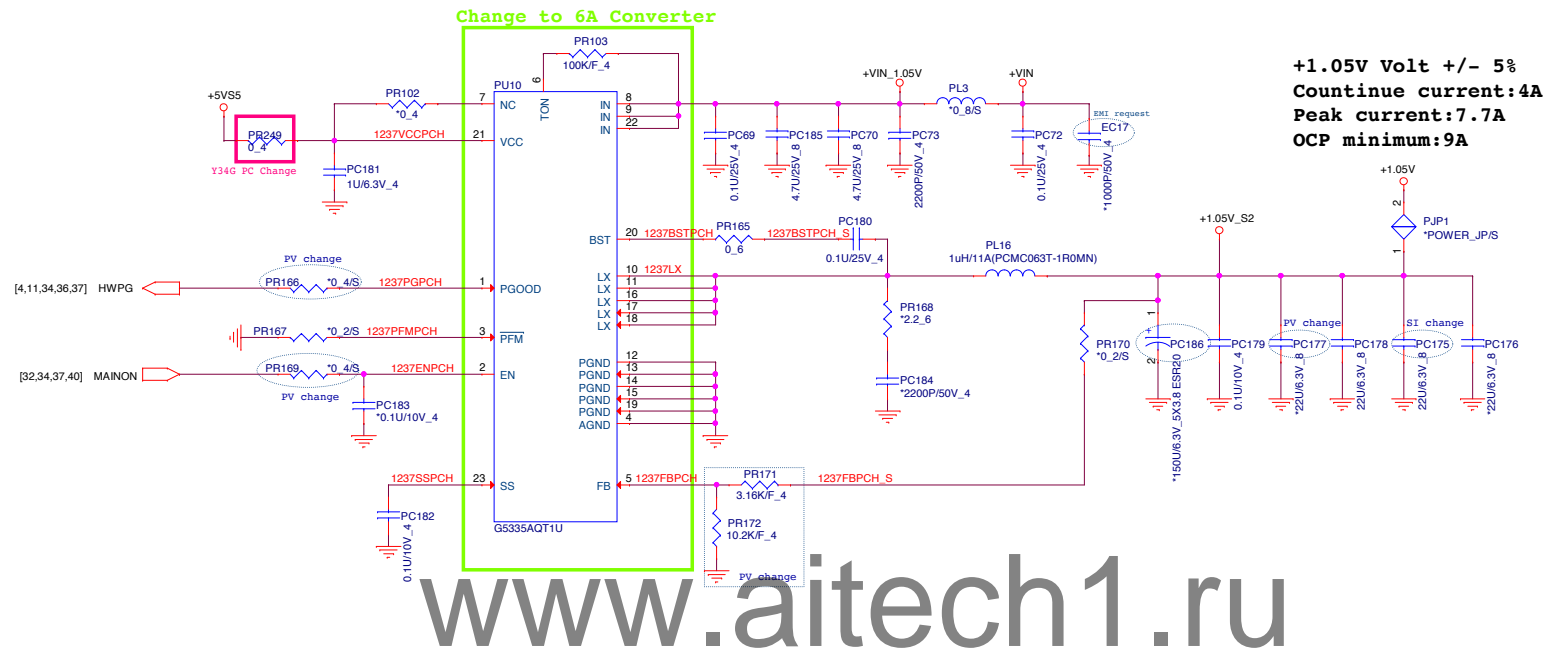
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff



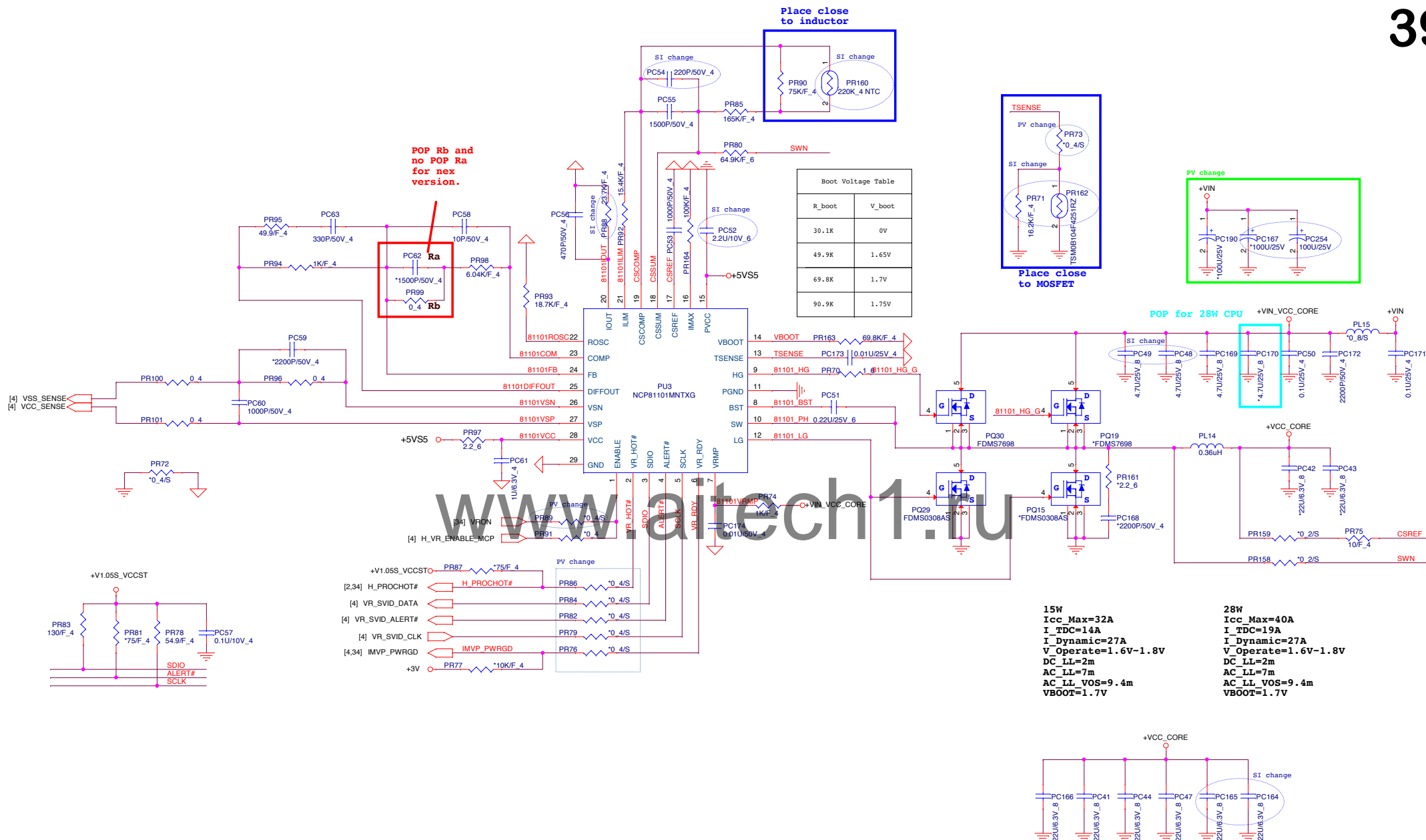


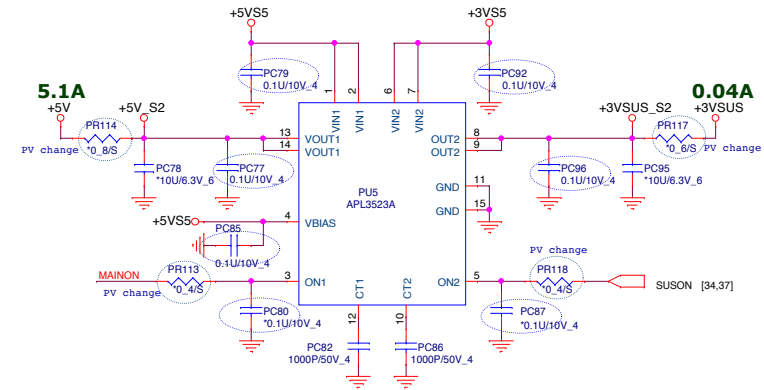
+1.35VSUS [2,4,12,13,29]

	<b>PROJECT : Y02</b>		
	<b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>DDR3 (RT8231A)/1.8VS5</b>	Rev 1A
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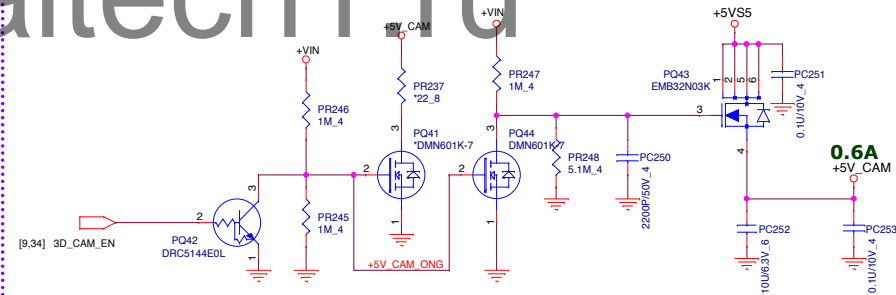



+VIN [24,26,29,30,35,36,37,39,40]  
+3VS5 [6,7,9,10,11,25,29,31,32,33,34,36,40]  
+5VS5 [13,25,29,32,36,37,39,40]






The schematic diagram illustrates the power supply circuit for the camera module. It features two main MOSFETs, PO42 and PO41, which are driven by the +VIN signal through a network of resistors (PR246, PR247, PR245, PR237) to generate the +5V\_CAM and +5V\_CAM\_ONG signals. A second MOSFET, PO43, is used to generate the +5V\_VS5 signal from a +5V\_VS5 input. The circuit includes several capacitors (PC251, PC250, PC252, PC253) and a diode (D1) to filter and regulate the output voltages. The output voltage for +5V\_CAM is specified as 0.6A.




	<b>PROJECT :U83</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>Dis-charge IC (SLG55448)</b>	Rev 1A
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	<b>PROJECT :U83</b> Quanta Computer Inc.				
	Size Custom	Document Number +VGACORE (RT8813A)			Rev 1A
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		<b>PROJECT :U83</b> Quanta Computer Inc.			
Size Custom	Document Number <b>+1.35V_VGA(A021237)</b>				Rev 1A
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		<b>PROJECT :U83</b> Quanta Computer Inc.	
		Size Custom	Document Number 1.05V_VGA/3V_VGA
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Battery Connector	Pavillion	ENVY
14"	DFAD08MR063	DFAD08MR064
15"	DFAD08MR065	DFAD08MR066
17"	DFFC20FR081	DFFC20FR081

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

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Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Tuesday, September 02, 2014	Sheet 44 of 44